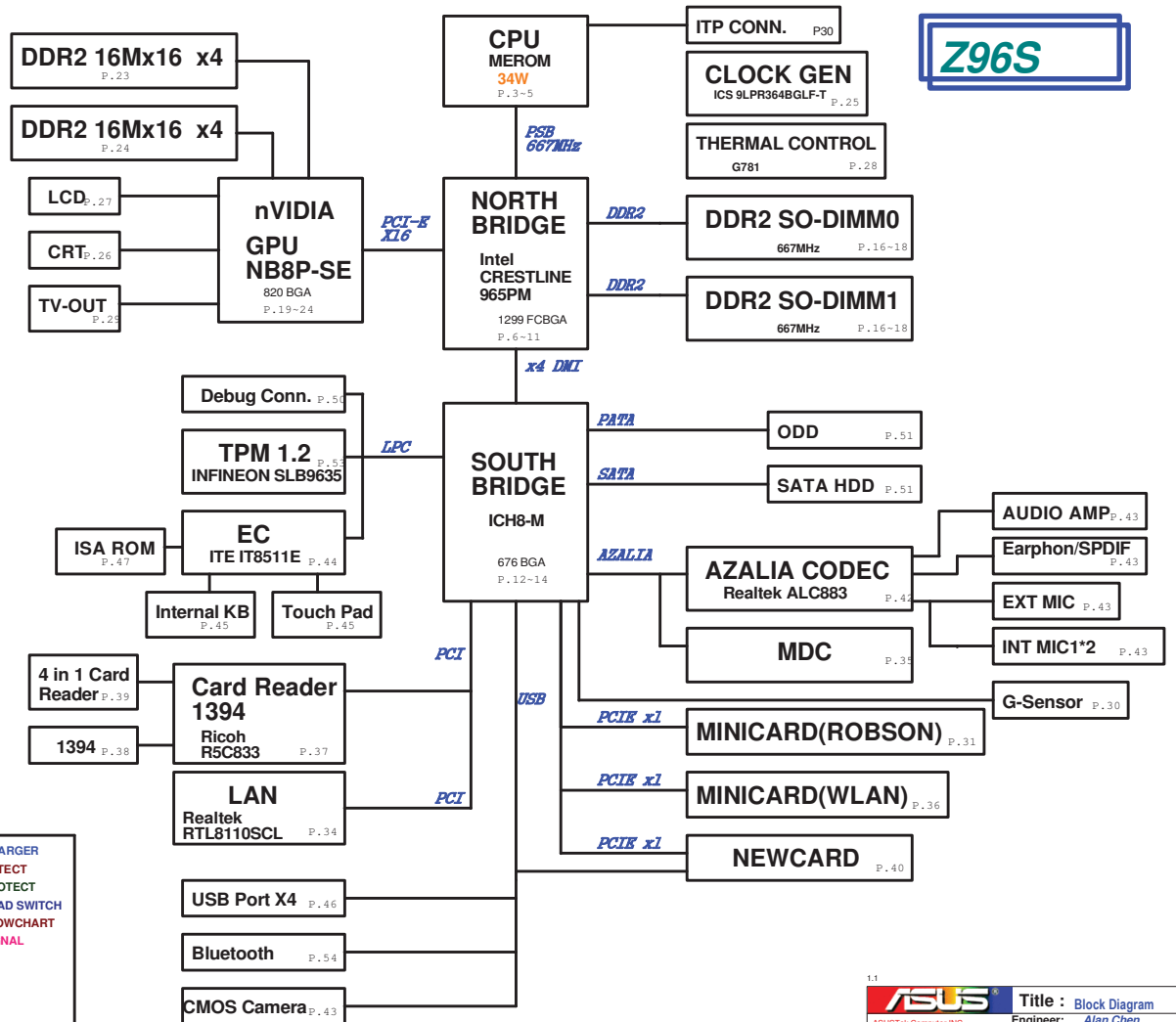


01_Block Diagram
 02_System Setting
 03_Merom CPU (1)
 04_Merom CPU (2)
 05_CPU CAPS.
 06_965PM-CPU (1)
 07_965PM-DDR2/PEG (2)
 08_965PM-DDR2 BUS (3)
 09_965PM-POWER (4)
 10_965PM-POWER (5)
 11_965PM-GND/STRAPPING (6)
 12_ICH8M(1)
 13_ICH8M(2)
 14_ICH8M(3)
 15_ICH8M-PEW/GND (4)
 16_DDR2 SO-DIMM0
 17_DDR2 SO-DIMM1
 18_DDR2 ADDRESS/TERMINATION
 19_VGA_nVIDIA_NB8P_MAIN(1)
 20_VGA_nVIDIA_NB8P_Mem/LVDS1(2)
 21_VGA_nVIDIA_NB8P_Mem/LVDS2(3)
 22_VGA_nVIDIA_NB8P_PCI-E/PWR(4)
 23_VGA_nVIDIA_NB8P_VRAM_A(5)
 24_VGA_nVIDIA_NB8P_VRAM_B(6)
 25_CLOCK_GEN-ICS9LPR364AGLF-T
 26_CRT CONNECTOR
 27_LVDS & INVERTER CONNECTOR
 28_THER SENSOR & FAN
 29_TV OUT CONN
 30_G-SENSOR & ITP
 31_MINI CARD - ROBSON
 32_SWITCH
 33_DISCHARGE
 34_GIGALAN-RTL8110SCL
 35_MDC&RJ45&RJ11
 36_MINI CARD - WLAN
 37_RICOH-R5C833_PCI
 38_RICOH-R5C833_1394/SD
 39_4 in 1 CARD READER
 40_NEWCARD
 41_Port Bar
 42_AUDIO-CODEC-ALC882
 43_AUDIO AMP & JACK
 44_EC-IT8511E
 45_Touch Pad/ KB
 46_USB CONN
 47_ISA ROM
 48_LED
 49_DCIN & BAT CONN
 50_Debug CONN.
 51_SATA-HDD & ODD
 52_SREW HOLE
 53_TPM CONNECTOR
 54_BT CONNECTOR
 55_POWER_VCORE
 56_POWER_SYSTEM_+3VO & +5VO
 57_POWER_1.5VS&1.05VS
 58_POWER_I/O_DDR & VTT
 59_POWER_+3VAO
 60_POWER_VGA_CORE
 61_POWER_CHARGER
 62_POWER_DETECT
 63_POWER_PROTECT
 64_POWER_LOAD SWITCH
 65_POWER_FLOWCHART
 66_POWER_SIGNAL
 67_HISTORY



EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BL_PWM_DA	O
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	CLK_PWRSERVE#	O
37	PWM3/GPA3	N/A	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	N/A	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GBP0	NUM_LED	O
154	TXD/GBP1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GBP3	SMB0_CLK	IO
164	SMDAT0/GBP4	SMB0_DAT	IO
5	GA20/GBP5	A20GATE	O
6	KBRST#/GBP6	RC_IN#	O
165	GPB7	THRO_CPU	O
47	CLKOUT/GPC0	N/A	
169	SMCLK1/GPC1	SMB1_CLK	IO
170	SMDAT1/GPC2	SMB1_DAT	IO
171	GPC3	Mail_LED	O
172	TMRI0/WU2/GPC4	AC_OK#	I
175	GPC5	OP_SD#	O
176	TMRI1/WU3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	N/A	
26	R1#(WU0/GPD0	SUSB#	I
29	R2#(WU1/GPD1	SUSC#	I
30	LPCRST#(WU4/GPD2	PLT_RST#	I
31	ECSCLK/GPD3	EXT_SC#	O
41	GPD4	RF_ON_SW#	O
42	GINT/GPD5	N/A	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	N/A	
87	ADC4/GPE0	EMAIL_SW#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	EXPLORE_SW#	I
90	ADC7/GPE3	DISTP_SW#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WU5/GPE5	N/A	
24	LPCPD#(WU6/GPE6	N/A	
25	CLKRUN#(WU7/GPE7	N/A	
101	GPJ2/DAC2	BL_DA	O
102	GPJ3/DAC3	BATSEL_2P#	O
81	GPK0/ADC0	P_PMON	I
22	ECSMI#(GPM0	EXT_SM#	O
116	PS2CLK2/GPF4	TP_CLK	IO
117	PS2DAT2/GPF5	TP_DAT	IO
118	PS2CLK3/GPF6	N/A	
119	PS2DAT3/GPF7	N/A	
113	FA16/GPG0	FA16	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	N/A	
3	FA20/GPG4	LID_EC#	I
4	FA21/GPG5	PMITHERM#	O
27	LPC80HL/GPG6	THRM_CPU#	I
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	I
55	GPH2	CPUPWR_GD#	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSC_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GP0	SB_PWRGD	O
149	GP1	N/A	
152	GP2	MCHOK	I
155	GP3	CHG_EN#	O
156	GP4	PRECHG	O
168	GP5	BAT_LL#	O
174	GP6	BAT_LEARN	O

ICH8-M GPIO SETTING

Pin	Pin Name	Signal Name	Type	Power_Well	Default
AG12	GPIO0/BMBUSY#	PM_BMBUSY#	IO	Core(To:3.3V)	GPI
AJ8	GPIO1/TACH1	VDDR_SELO	IO	Core(To:3.3V)	GPI
F8	GPIO2/PIROE#	INT_SHIFT_LOW#	IO	Core(To:5V)	GPI
G11	GPIO3/PIROF#	INT_SHIFT_HIGH#	IO	Core(To:5V)	GPI
F12	GPIO4/PIROG#	PCL_INTG#	IO	Core(To:5V)	GPI
B3	GPIO5/PIROH#	PCL_INTH#	IO	Core(To:5V)	GPI
AJ9	GPIO6/TACH2	VDDR_SEL1	IO	Core(To:3.3V)	GPI
AH9	GPIO7/TACH3	VDDR_SEL2	IO	Core(To:3.3V)	GPI
AE16	GPIO8	EXT_SM#	IO	SUS(To:3.3V)	GPI
AG19	GPIO9/WOL_EN	TP	IO	SUS(To:3.3V)	GPI
AJ24	GPIO10/CLGPIO1	TP	IO	SUS(To:3.3V)	GPI
AG22	SMBALERT#(GPIO11	NC	IO	SUS(To:3.3V)	Native
AC19	GPIO12	EXT_SC#	IO	SUS(To:3.3V)	GPI
AH21	GPIO13/GLAN_DOCL#	NC	IO	SUS(To:3.3V)	Native
AF22	GPIO14/CLGPIO2	TP	IO	SUS(To:3.3V)	GPI
AE20	GPIO15/STP_PCI#	STP_PCI#	IO	SUS(To:3.3V)	Native
AJ14	GPIO16/DPRSLPVR	PM_DPRSLPVR	IO	Core(To:3.3V)	Native
AG8	GPIO17/TACH0	PM_EXTTS#0	IO	Core(To:3.3V)	GPI
AH12	GPIO18	VCORE_SELO	IO	Core(To:3.3V)	GPO
AJ10	GPIO19/SATA1GP	CB_SD#	IO	Core(To:3.3V)	GPI
AE11	GPIO20	VCORE_SEL1	IO	Core(To:3.3V)	GPO
AJ12	GPIO21/SATA0GP	WLAN_BT_LED_EN#	IO	Core(To:3.3V)	GPI
AG10	GPIO22/SCLOCK	TP	IO	Core(To:3.3V)	GPI
E6	GPIO23/LDRQ1#	TP	IO	Core(To:3.3V)	Native
AJ27	GPIO24/CLGPIO0	TP	IO	SUS(To:3.3V)	GPO
AG18	GPIO25/STP_CPU#	STP_CPU#	IO	SUS(To:3.3V)	Native
AH27	GPIO26/S4_STATE#	TP	IO	SUS(To:3.3V)	Native
AH25	GPIO27/QRT_STATE#	VGMCH_SELO	IO	SUS(To:3.3V)	GPO
AD16	GPIO28/QRT_STATE1	VGMCH_SEL1	IO	SUS(To:3.3V)	GPO
AG17	GPIO29/OC#5	USB_OC#5	IO	SUS(To:3.3V)	Native
AD12	GPIO30/OC#6	NEWCARD_OC#	IO	SUS(To:3.3V)	Native
AJ18	GPIO31/OC#7	USB_OC#7	IO	SUS(To:3.3V)	Native
AH11	GPIO32/CLKRUN#	PM_CLKRUN#	IO	Core(To:3.3V)	Native
AE10	GPIO33/HDA_DOCK_EN#	TP	IO	Core(To:3.3V)	GPO
AG14	GPIO34/HDA_DOCK_RST#	TP	IO	Core(To:3.3V)	GPO
AG13	GPIO35/SATACLKREQ#	VGPU_SEL1	IO	Core(To:3.3V)	GPO
AF11	GPIO36/SATA2GP	WLAN_ON#	IO	Core(To:3.3V)	GPI
AG11	GPIO37/SATA3GP	BT_ON#	IO	Core(To:3.3V)	GPI
AF9	GPIO38/SLOAD	PM_EXTTS#1	IO	Core(To:3.3V)	GPI
AJ11	GPIO39/SDATAOUT0	CLK_PWRSERVE#	IO	Core(To:3.3V)	GPI
AG16	GPIO40/OC#1#	USB_CON_OC0#1	IO	SUS(To:3.3V)	Native
AG15	GPIO41/OC#2#	USB_CON_OC2#3	IO	SUS(To:3.3V)	Native

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	REQ#0/GNT#0	INTB-->INTB
1394	AD17	REQ#0/GNT#0	INTA-->INTA
LAN	AD23	REQ#2/GNT#2	INTA-->INTC

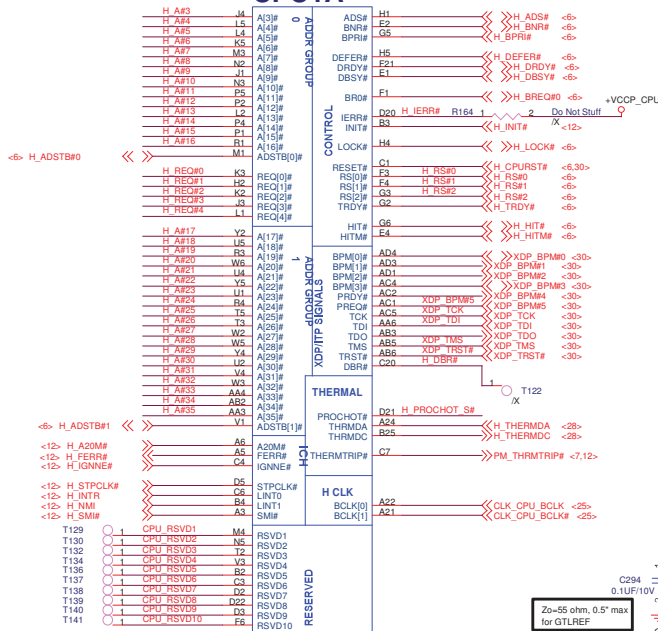
SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)

Pin	Pin Name	Signal Name	Type	Power_Well	Default
AD16	GPIO42/OC3#	USB_CON_OC23#	IO	SUS(To:3.3V)	Native
AG17	GPIO43/OC4#	USB_CON_OC4#	IO	SUS(To:3.3V)	Native
N/A	GPIO44	N/A	IO	N/A	N/A
N/A	GPIO45	N/A	IO	N/A	N/A
N/A	GPIO46	N/A	IO	N/A	N/A
N/A	GPIO47	N/A	IO	N/A	N/A
AD10	GPIO48/SDATAOUT1	TP	IO	Core(To:3.3V)	GPI
AG29	GPIO49/CPUPWRGD	H_PWRGD	IO	V_CPU_IO	Native
E18	GPIO50/REQ1#	PCL_REQ#1	IO	Core(To:5.5V)	Native
C18	GPIO51/GNT1#	TP	IO	Core(To:3.3V)	Native
B19	GPIO52/REQ2#	PCL_REQ#2	IO	Core(To:5.5V)	Native
F18	GPIO53/GNT2#	PCL_GNT#2	IO	Core(To:3.3V)	Native
A11	GPIO54/REQ3#	PCL_REQ#3	IO	Core(To:5.5V)	Native
C10	GPIO55/GNT3#	NC	IO	Core(To:3.3V)	Native

1.1

		Title : System Setting Engineer: Alan Chen	
Size	Project Name	Rev	
Custom	296S	2.0	
Date	2007-11-30	Sheet	2 of 67

CPU1A

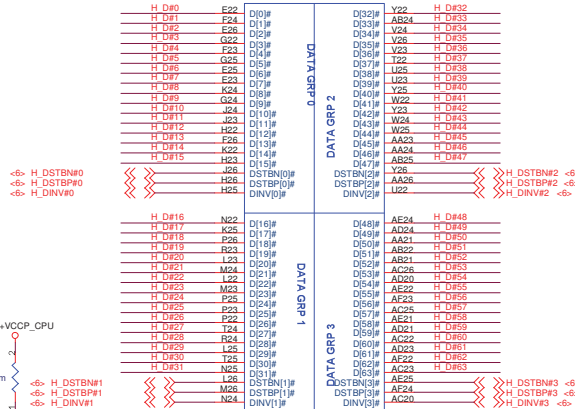


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<< H_A[35:3] << H_A[35:3]

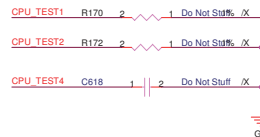
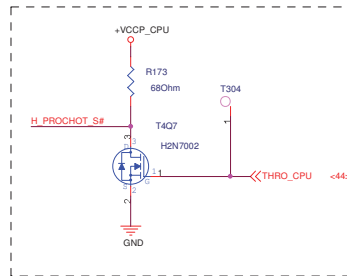
<< H_REQ[4:0] << H_REQ[4:0]

CPU1B

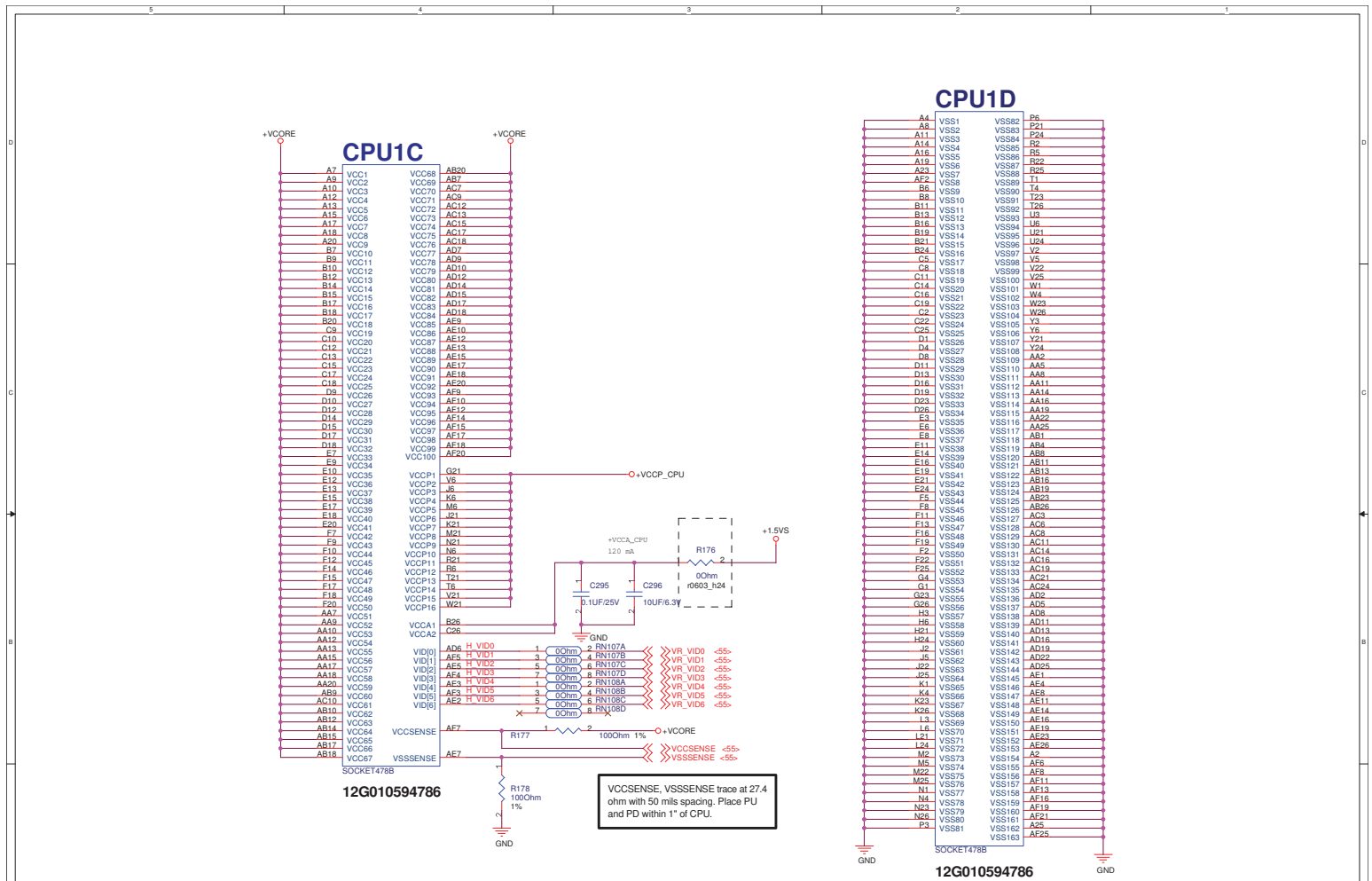


Comp0.2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".

Comp.1.3 connect with Zo=55 ohm, make trace length shorter than 0.5".



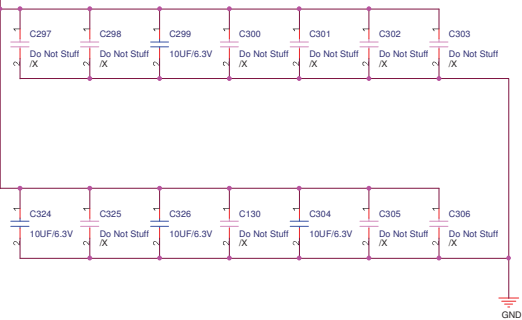
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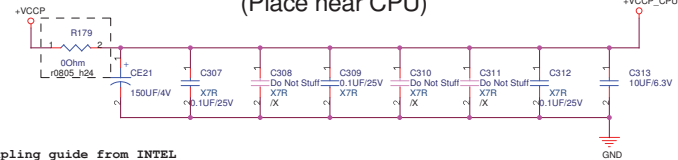
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+V_{Core}

44A for Merom



+V_{CCP} Decoupling Capacitor (Place near CPU)

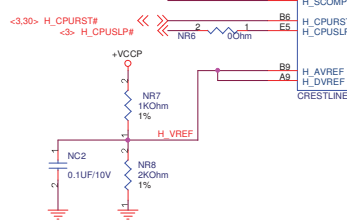


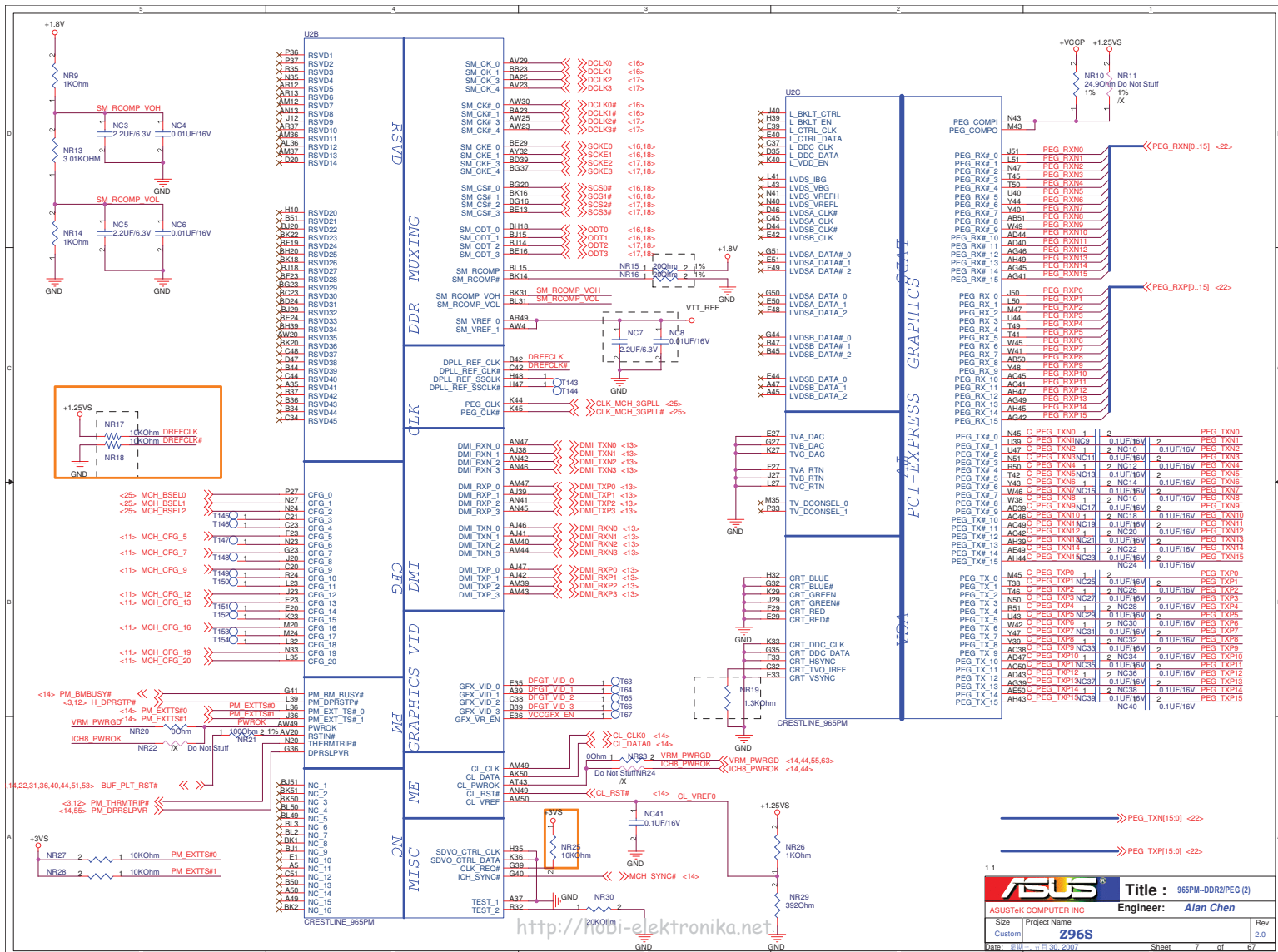
Decoupling guide from INTEL

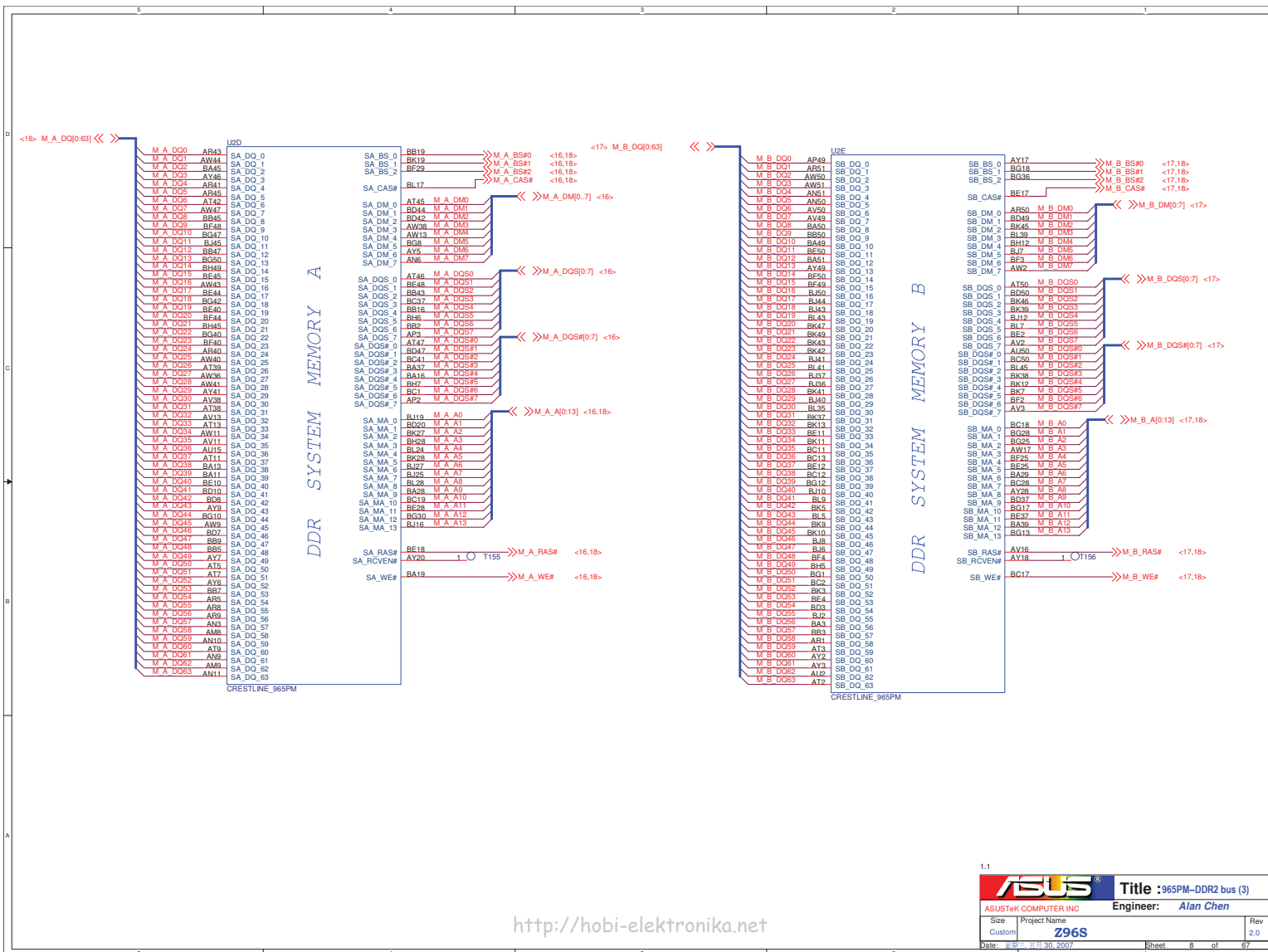
V _{Core}	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
V _{CCP}	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

1.1

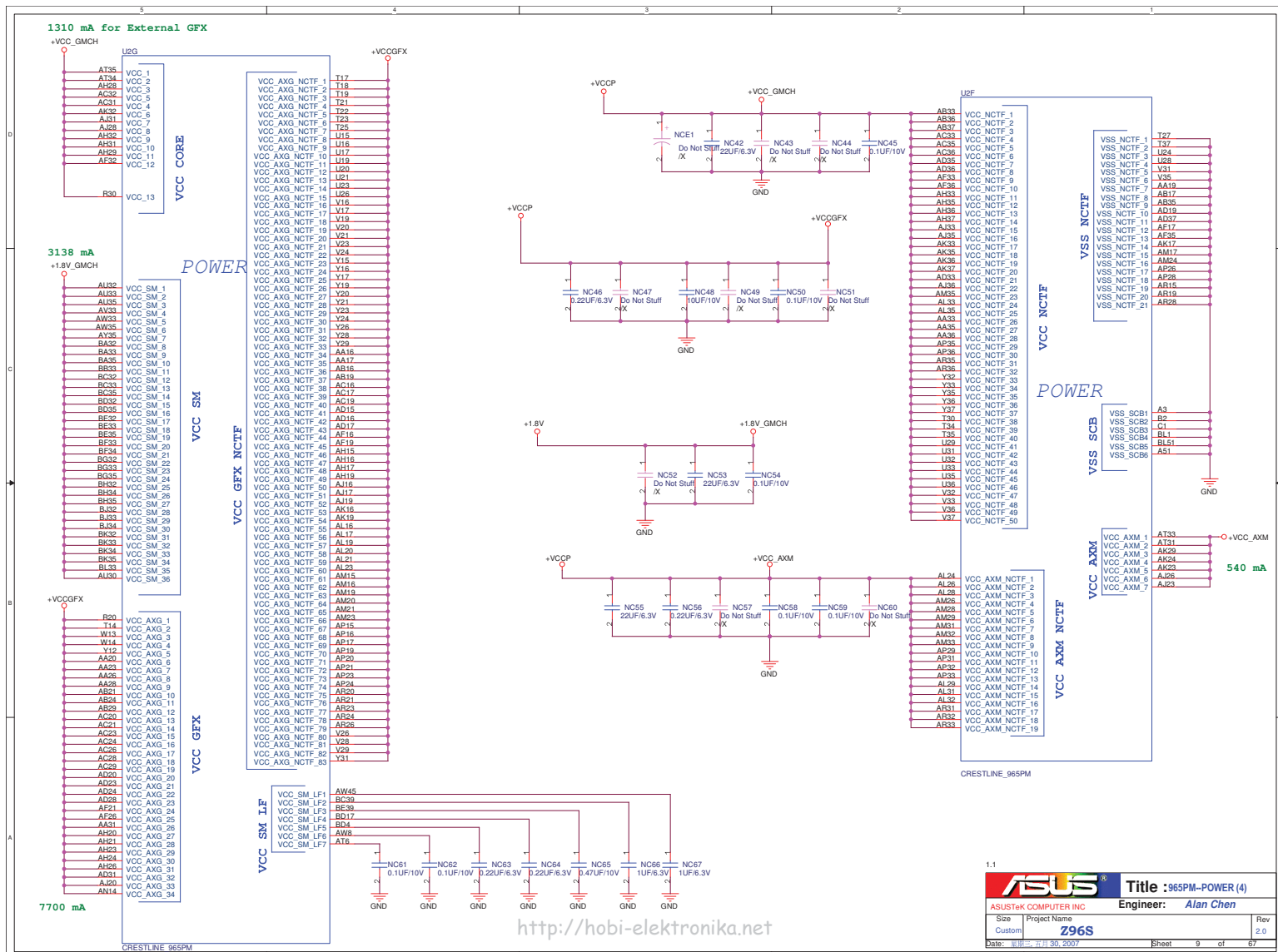
ASUS		Title : CPU CAP and HOLES	
ASUSTek COMPUTER INC. NB1		Engineer: Alan Chen	
Size	Project Name	Rev	
Custom	Z96S	2.0	
Date: 2007-07-11 30, 2007		Sheet	5 of 67

[illegible]

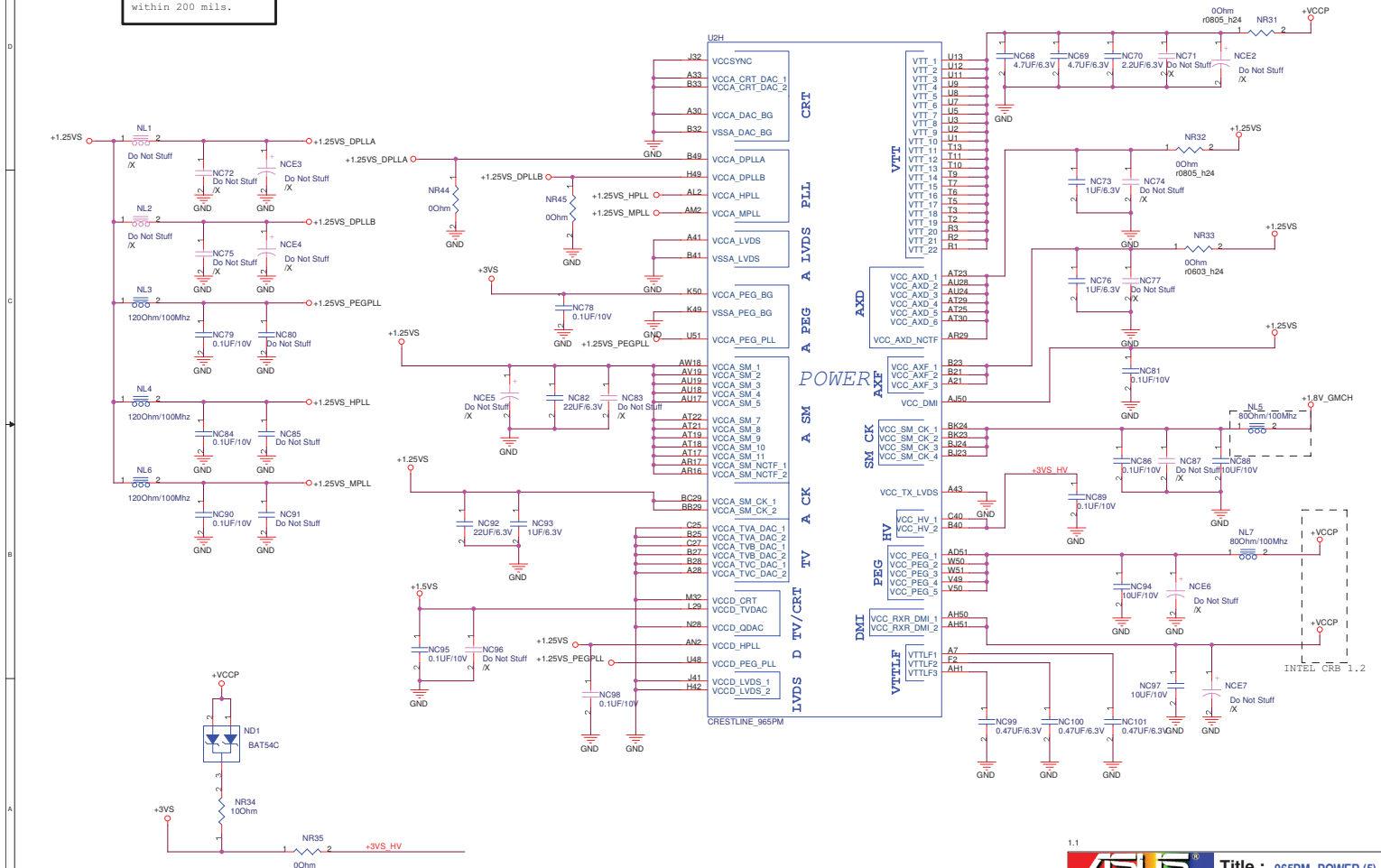




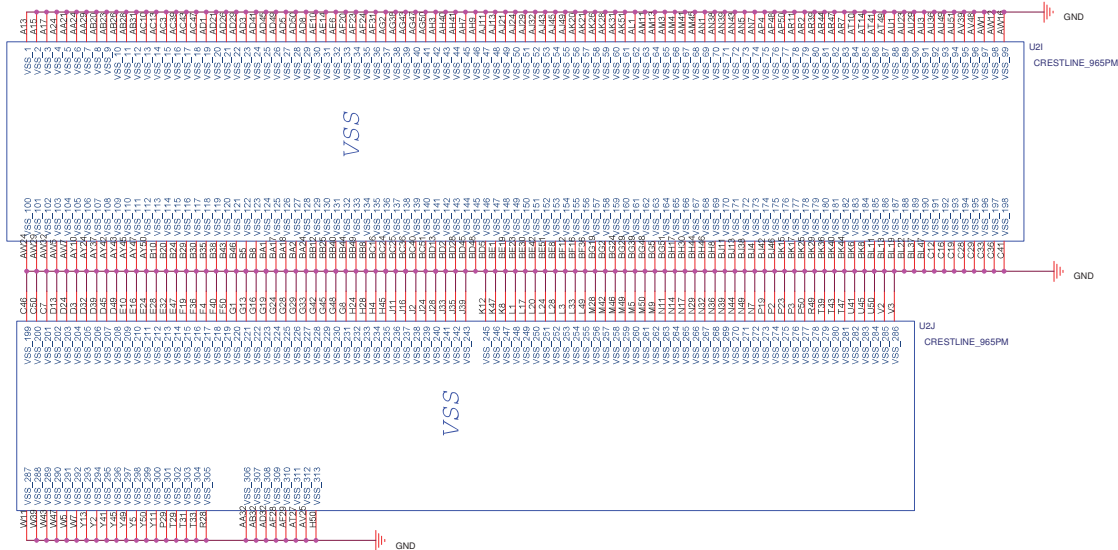
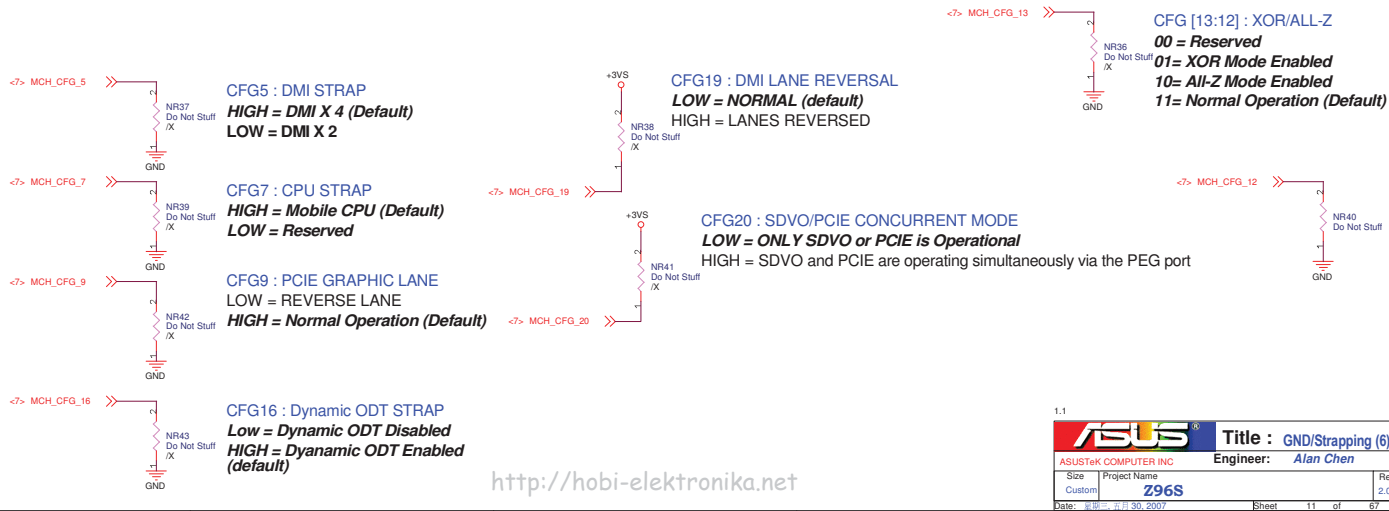
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NOTE: 0.1uF caps in 1.5VS_XPLL need to be located as edge caps within 200 mils.

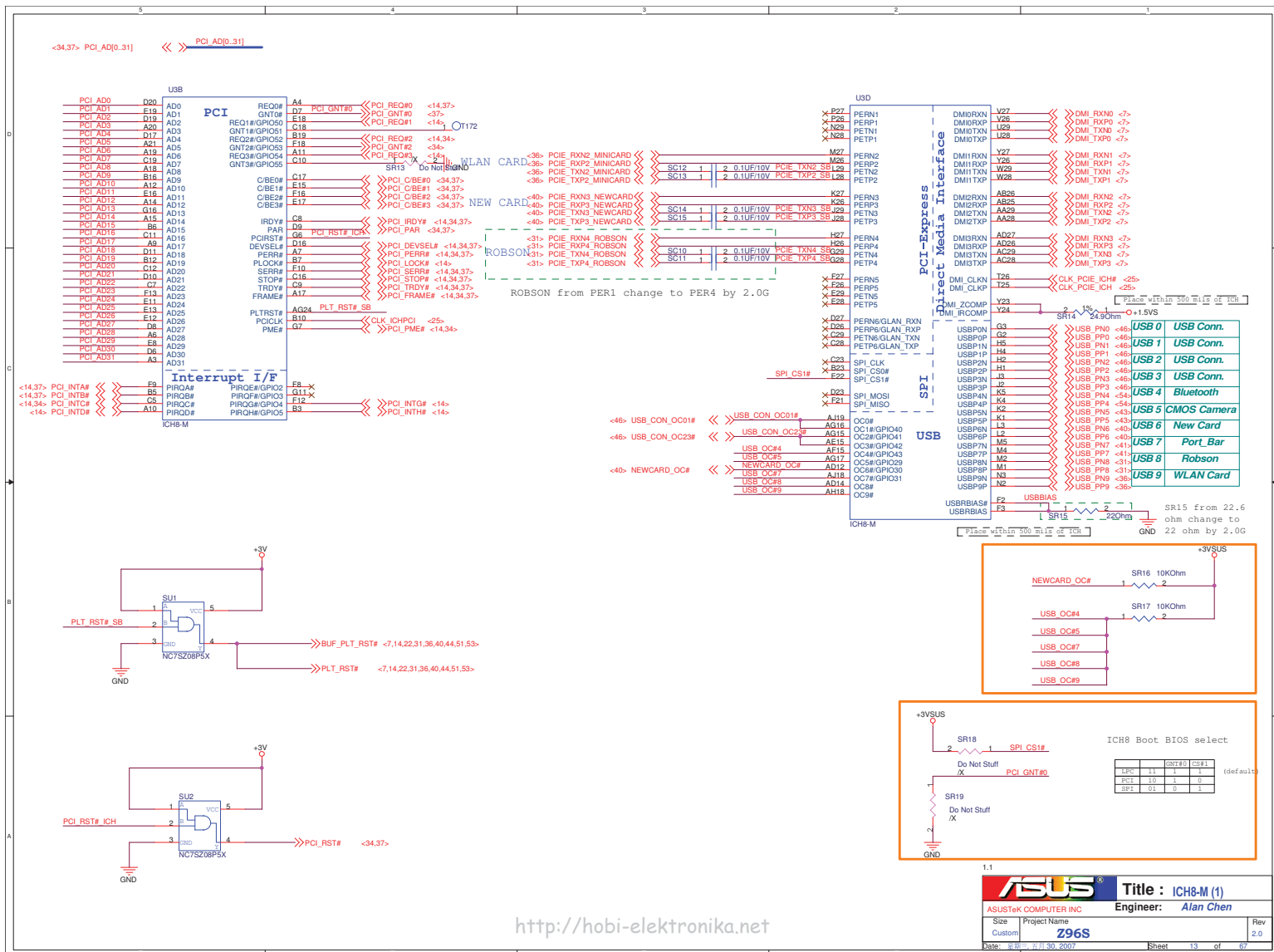


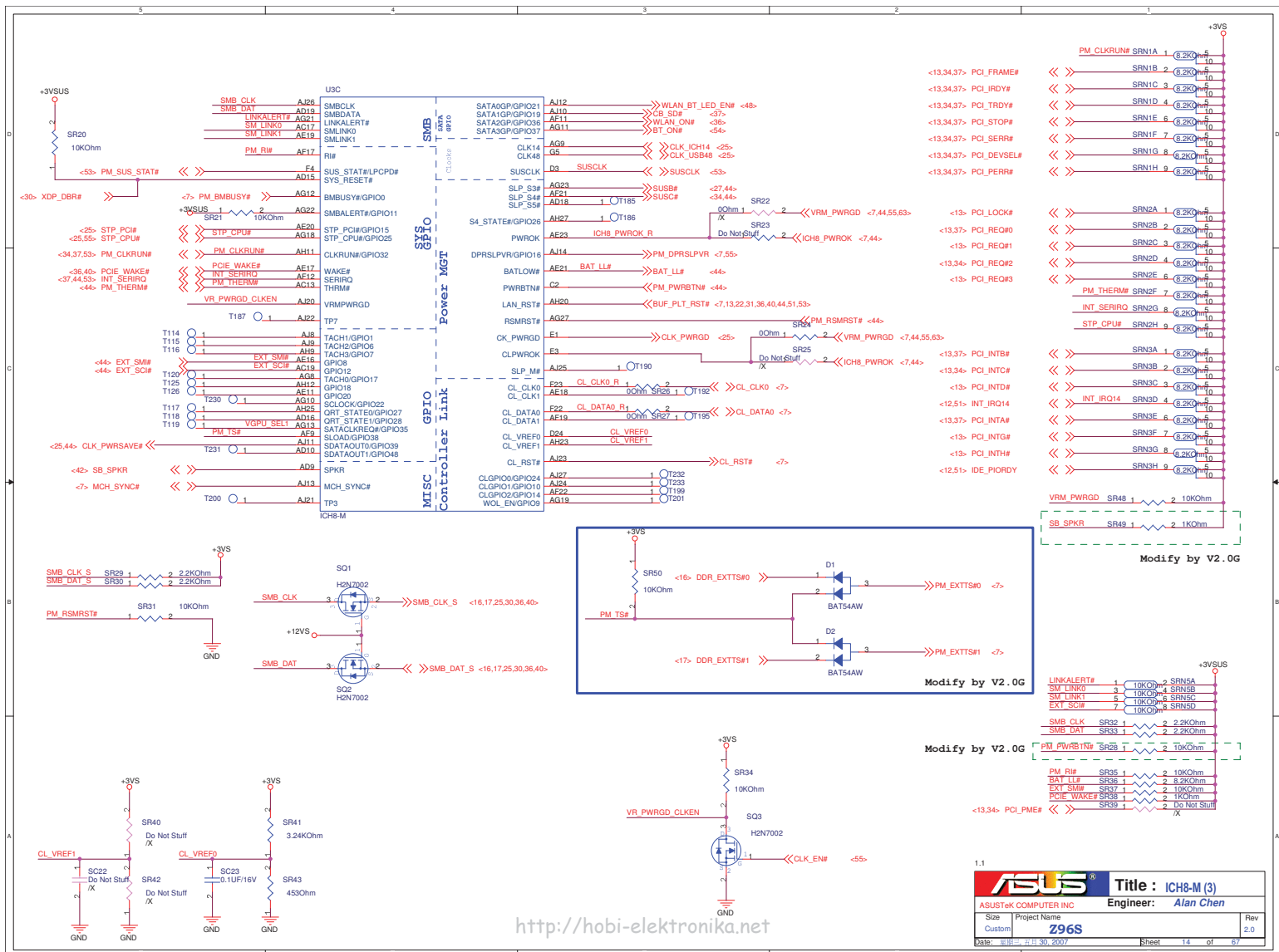
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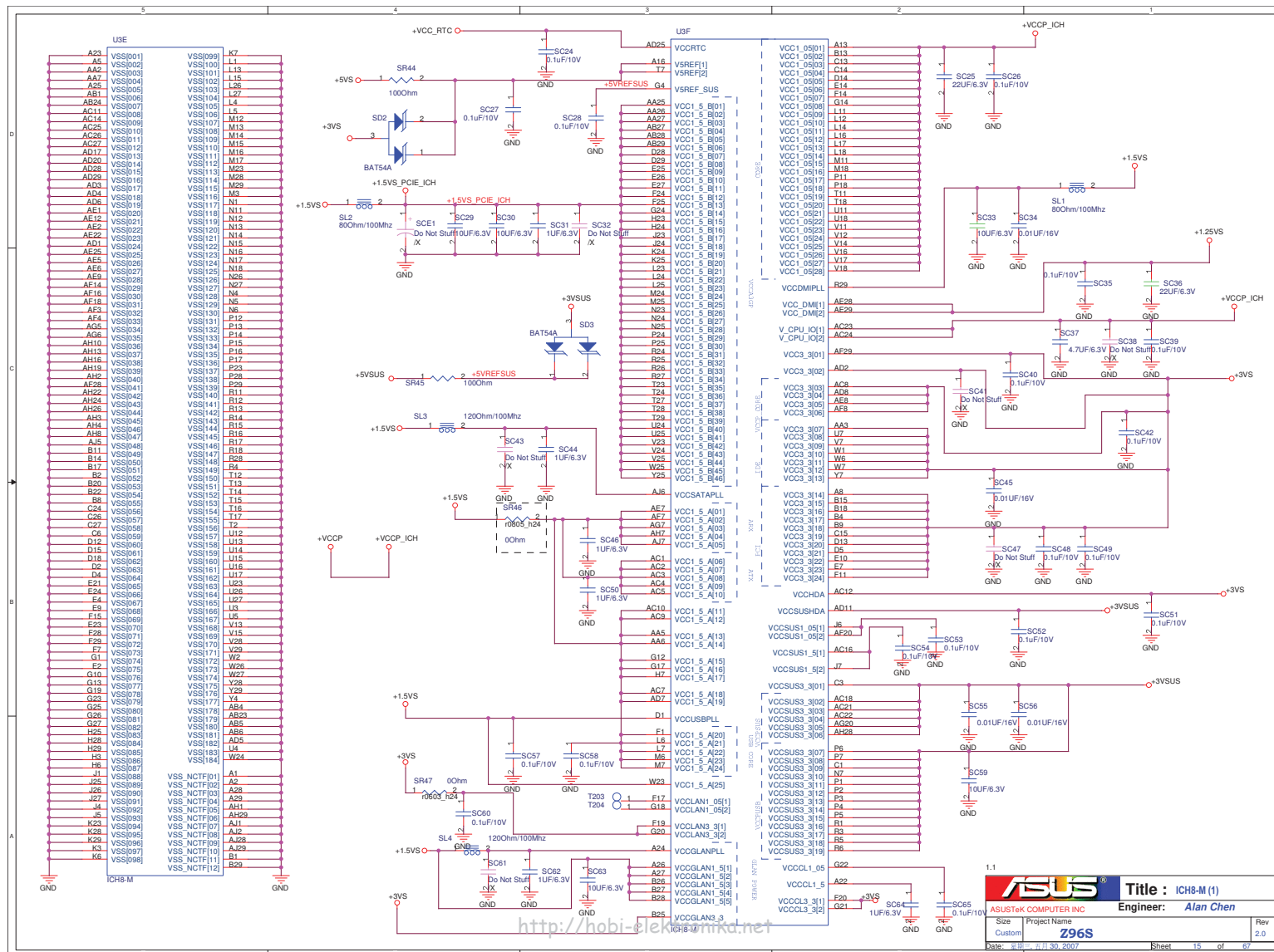


1.1

ASUS		Title : GND/Strapping (6)	
ASUSTeK COMPUTER INC.		Engineer: Alan Chen	
Size	Project Name	Rev	
Custom	Z96S	2.0	
Date: 2007-11-30, 2007	Sheet	11	of 67







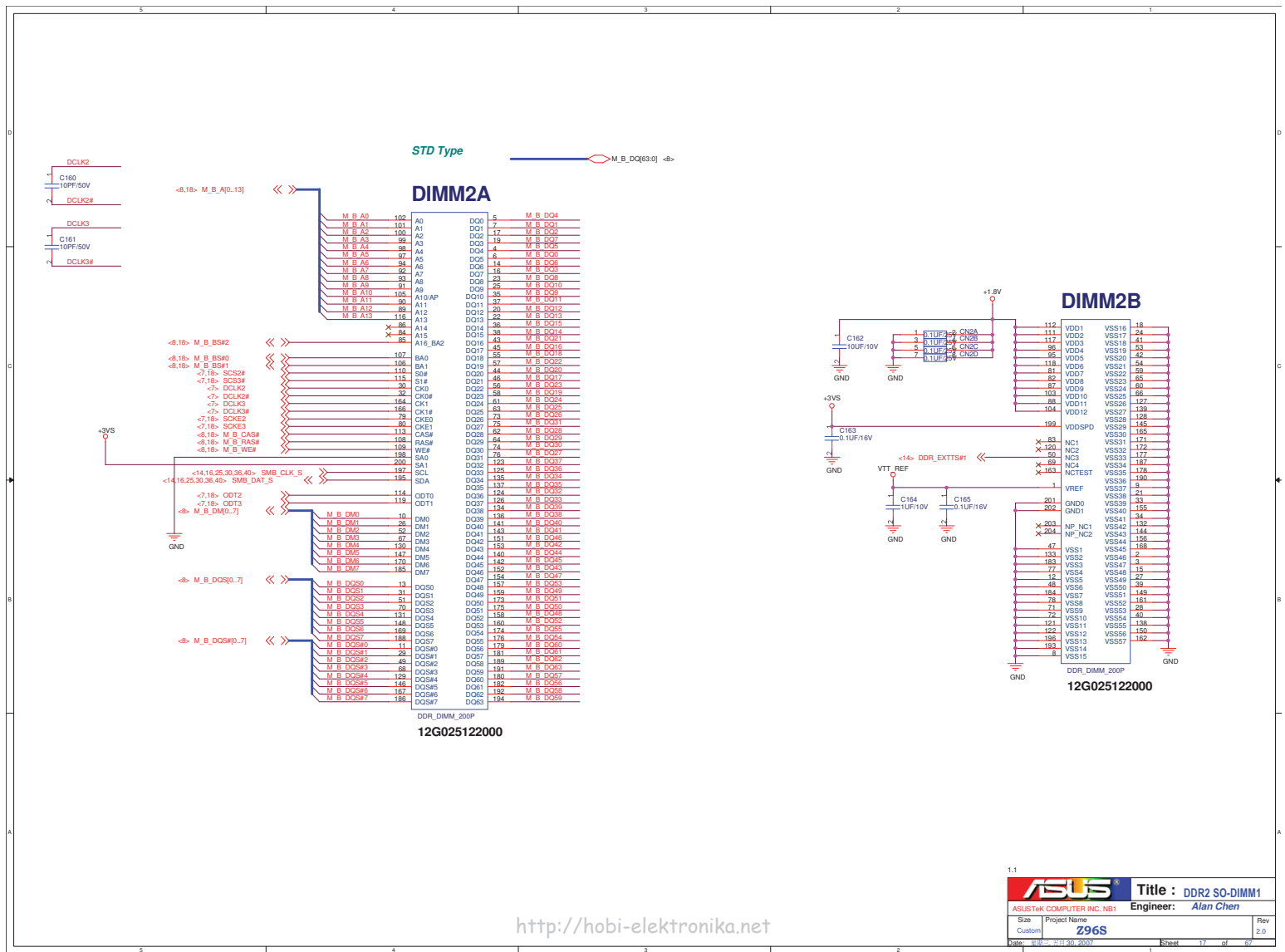
REV Type

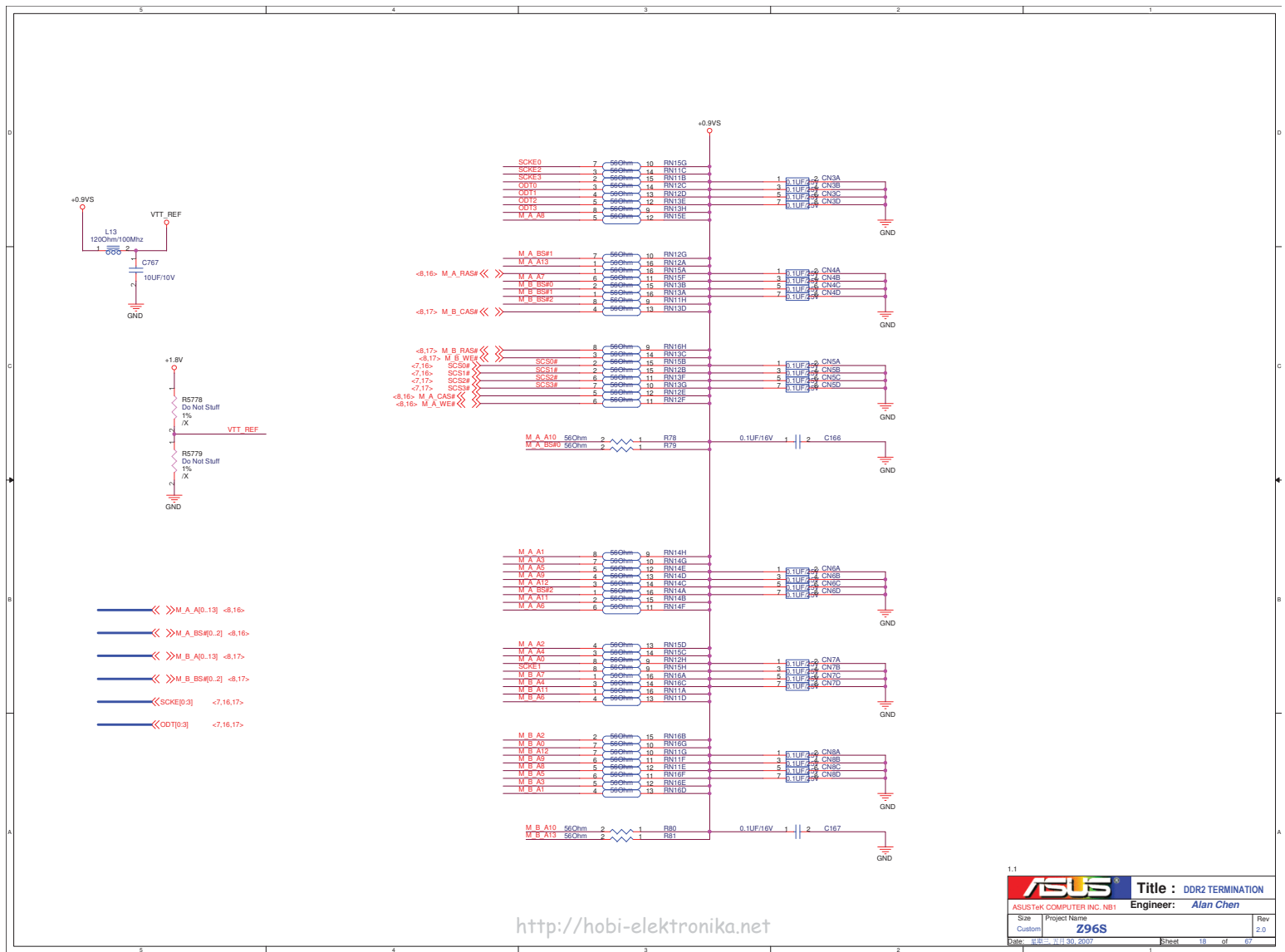
DIMM1A

12G025332003

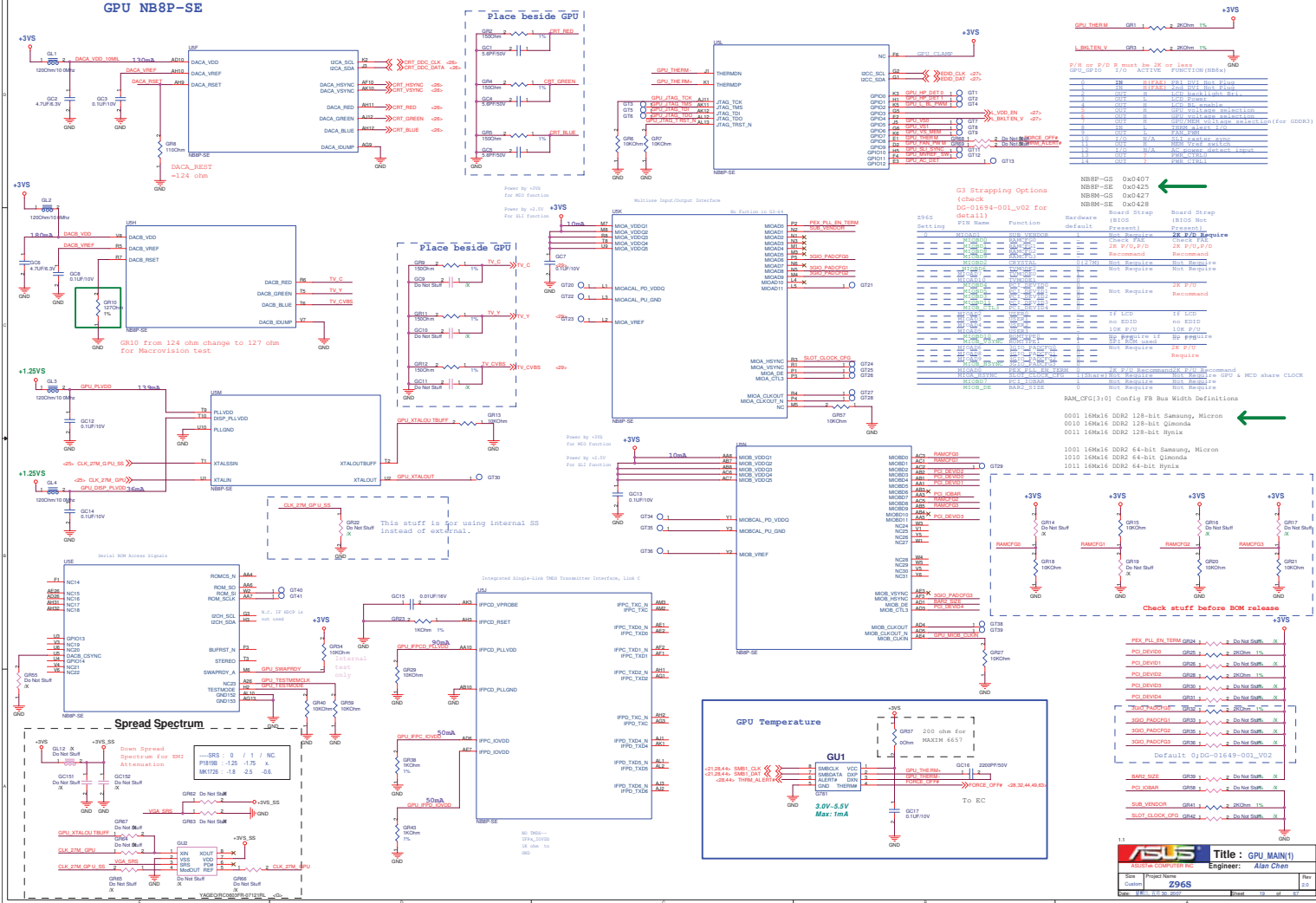
DIMM1B

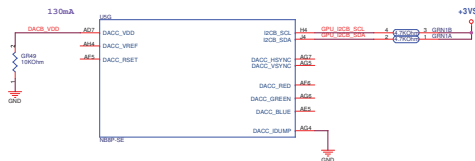
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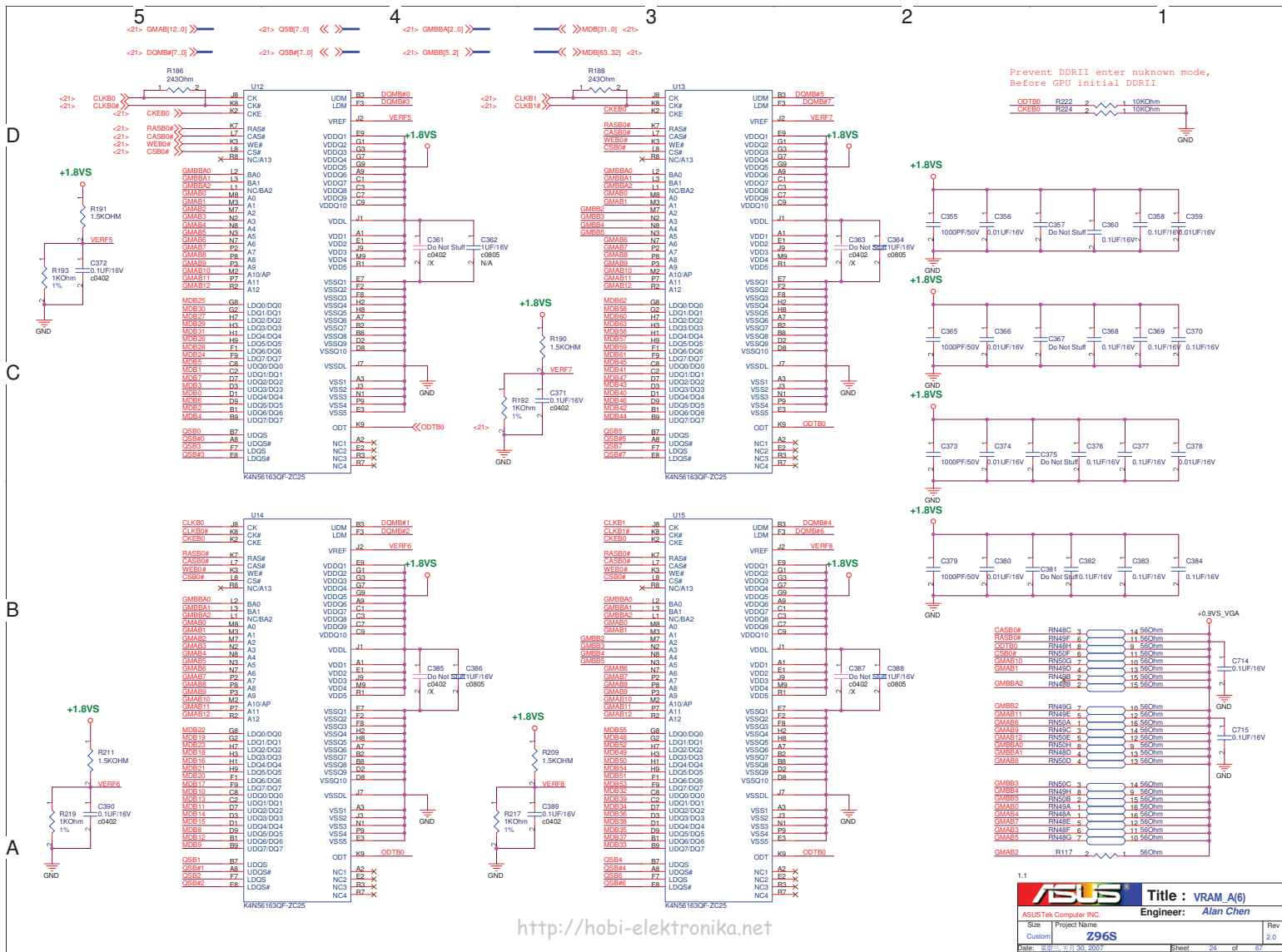


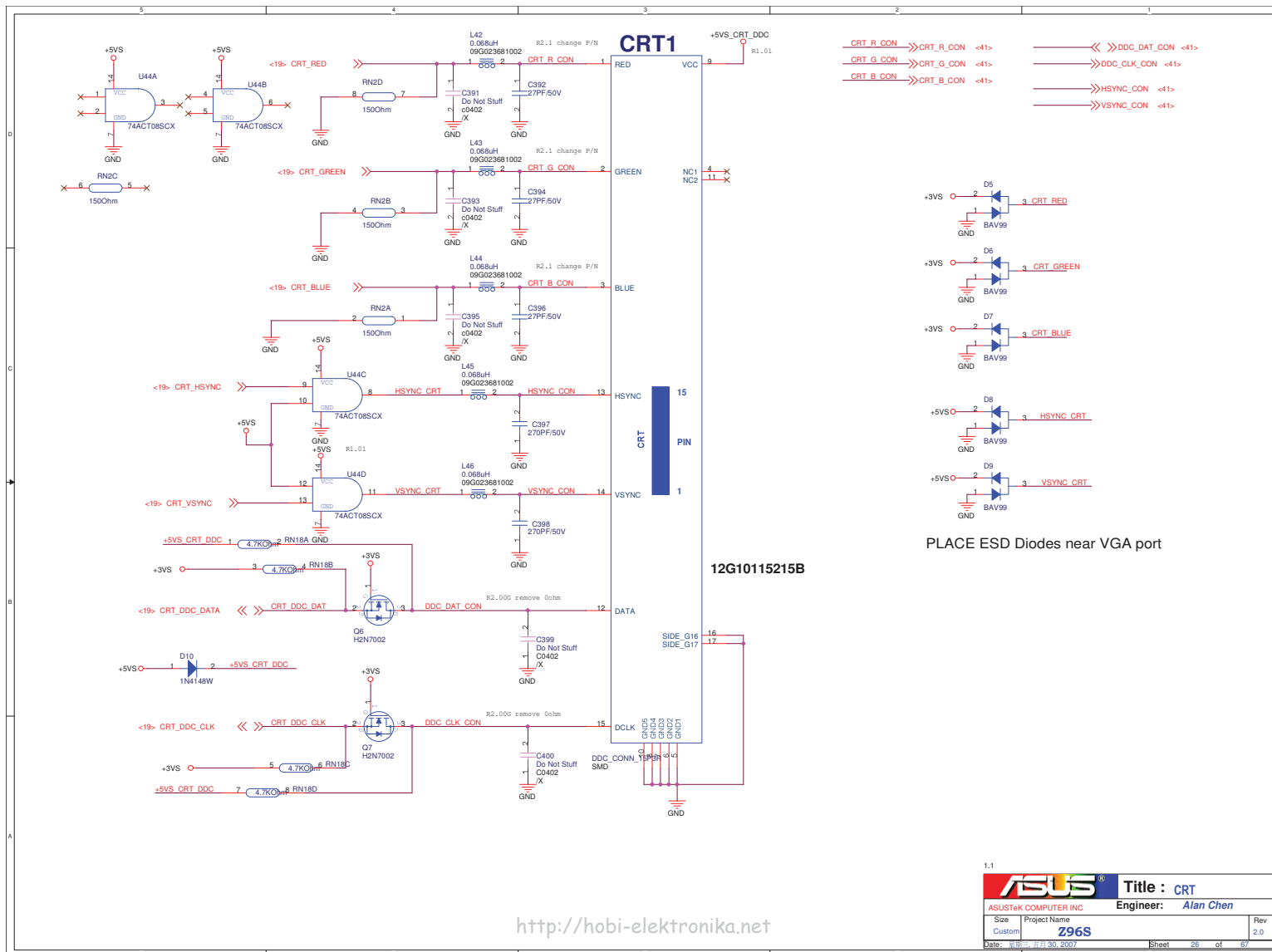
GPU NB8P-SE









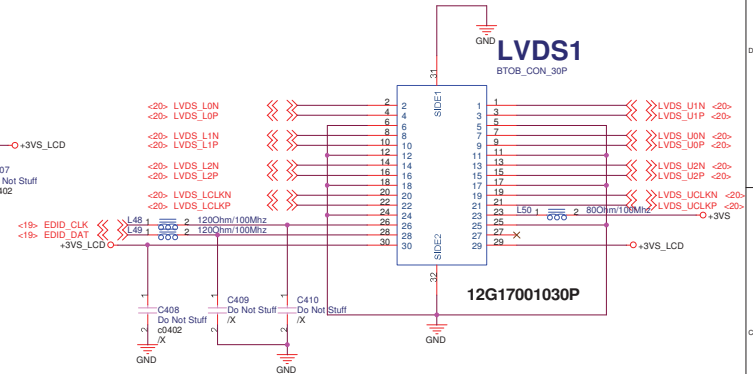


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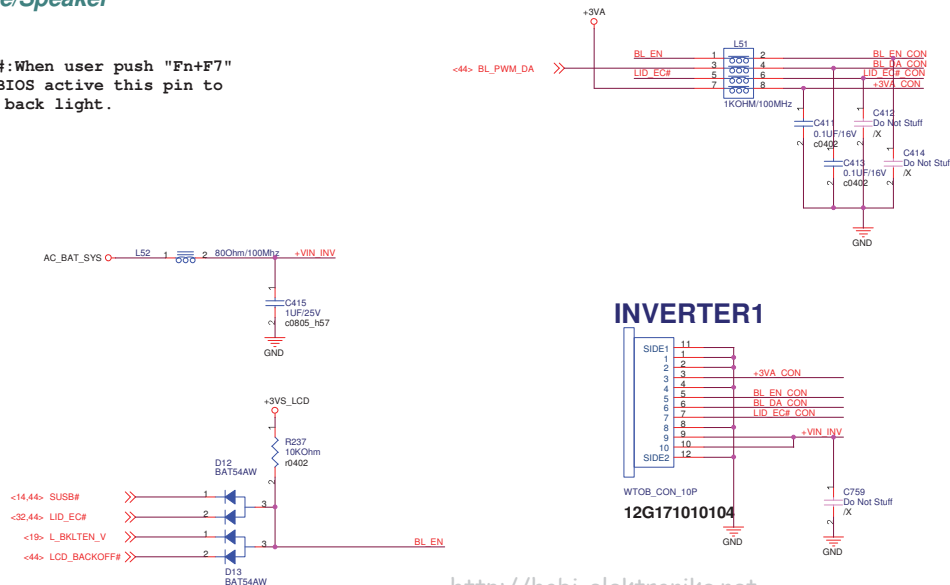
ASUS		Title : CRT	
ASUSTek COMPUTER INC		Engineer: Alan Chen	
Size	Project Name	Rev	
Custom	Z96S	2.0	
Date: 2007-11-30	Sheet: 26	of: 67	

LCD LVDS Interface

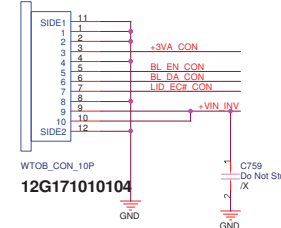
Cable Requirement:
Impedance: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"



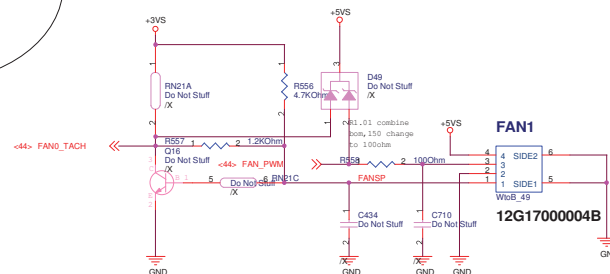
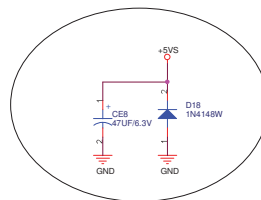
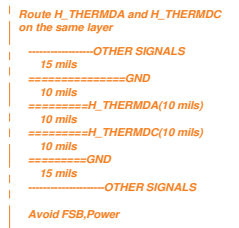
BIOS
BACK_OFF#:When user push "Fn+F7"
button, BIOS active this pin to
turn off back light.



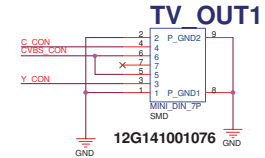
INVERTER1



DC FAN Control



CPU FAN will be forced on:
1) Thermal Sensor Over-temperature
2) WATCHDOG asserted by EC



5

4

3

2

1

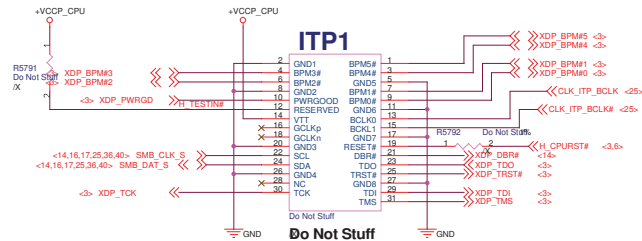
D

C

B

A

ITP

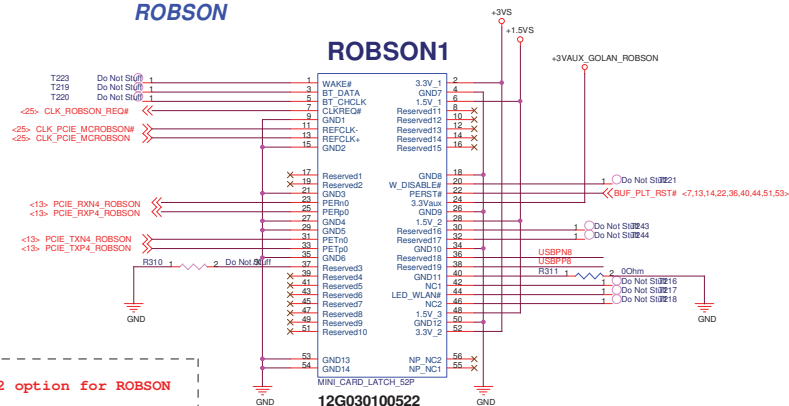

<http://hobi-elektronika.net>

1.1

ASUS		Title : ITP	
ASUSTek Computer INC.		Engineer: Alan Chen	
Size	Project Name	Rev	
Custom	Z96S	2.0	
Date: 2017-11-30 20:07	Sheet	30	of 60

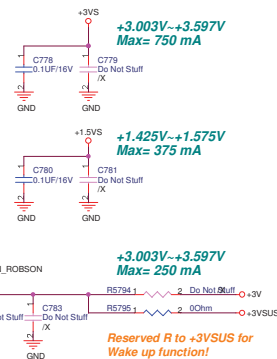
ROBSON

ROBSON1



ES1 & ES2 option for ROBSON

	ES1	ES2
R310	N/A	Mount
R311	Mount	N/A



+3.003V~+3.597V
Max= 750 mA

+1.425V~+1.575V
Max= 375 mA

+3.003V~+3.597V
Max= 250 mA

Reserved R to +3VSUS for Wake up function!

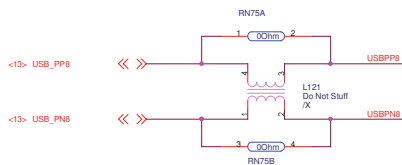
12G030100522
H = 4.0mm

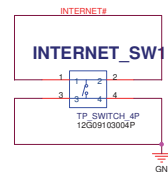
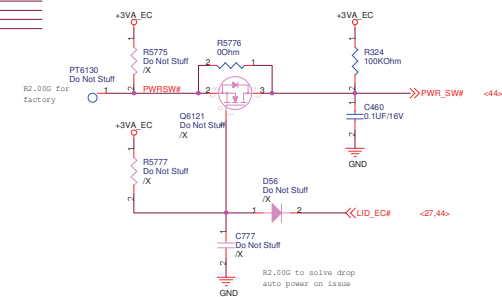
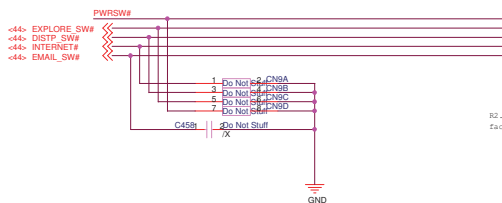
D

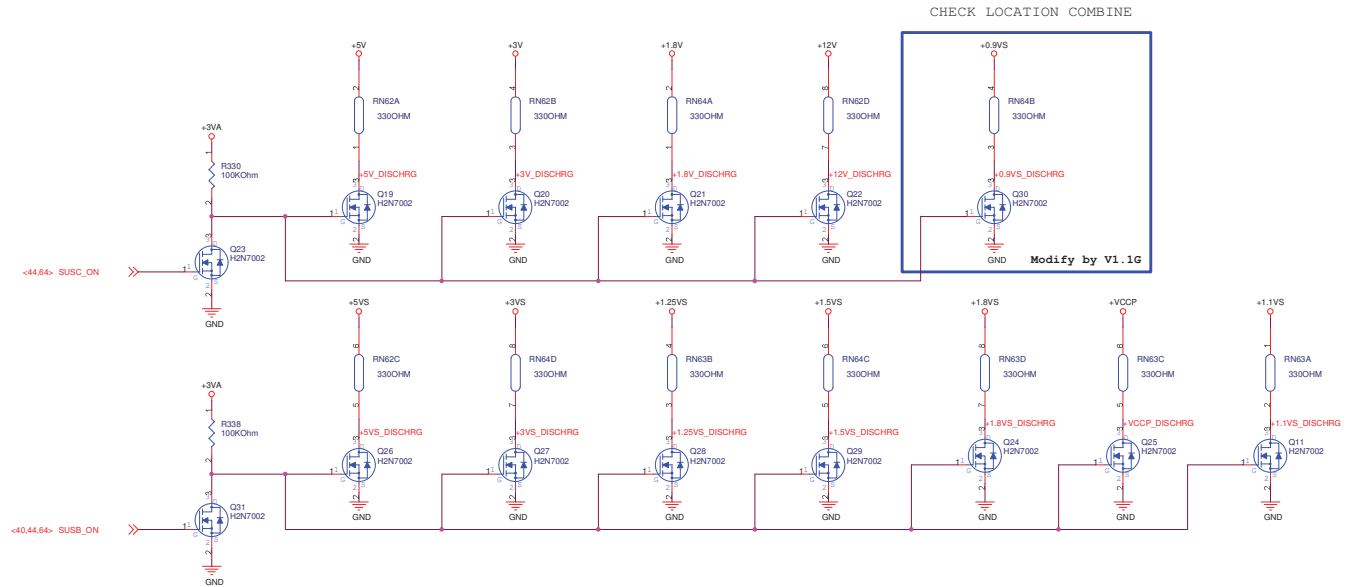
C

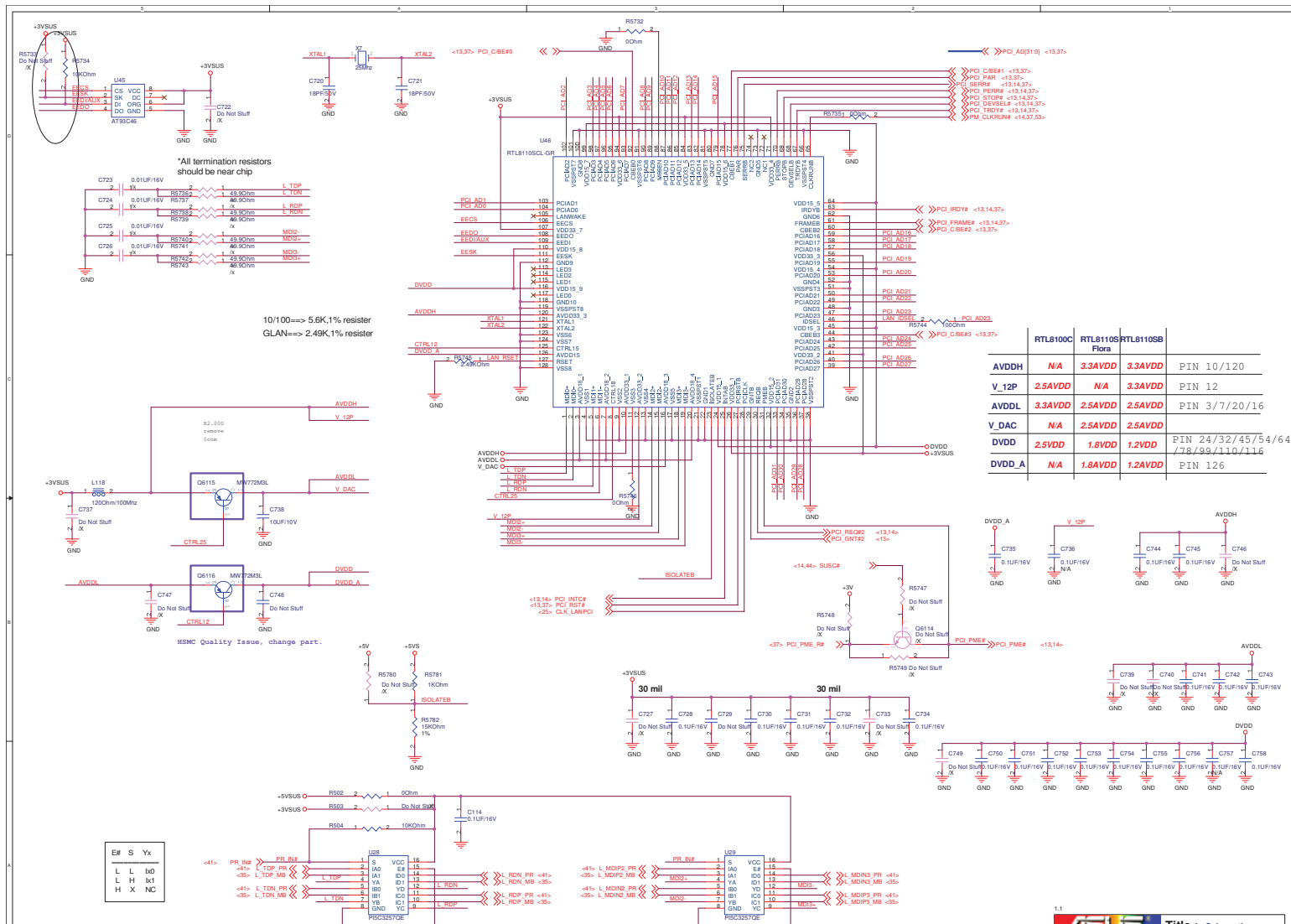
B

A

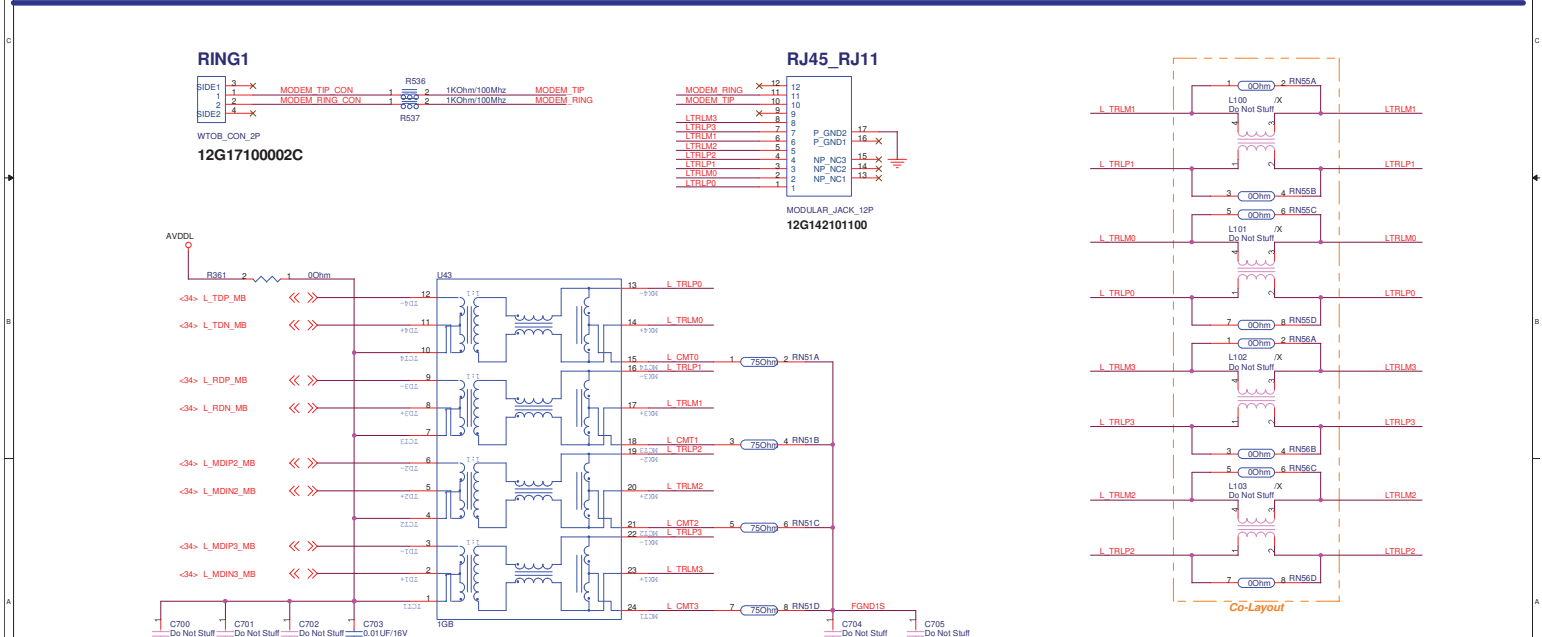


[illegible]

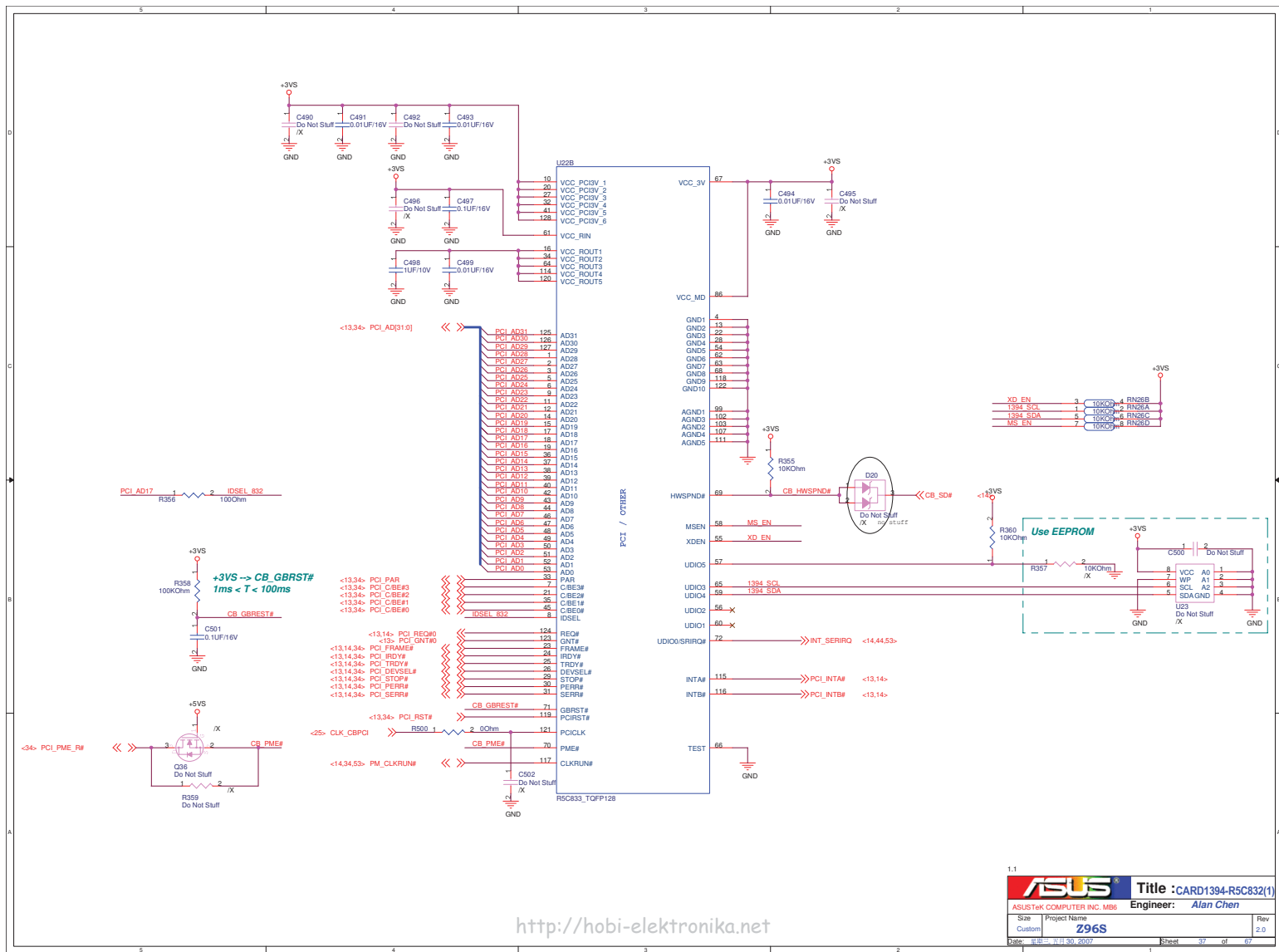


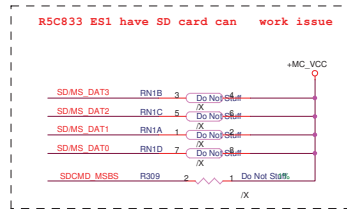


	RTL8100C	RTL8110S	RTL8105B	
	Flora			
AVDDH	N/A	3.3AVDD	3.3AVDD	PIN 10/120
V_12P	2.5AVDD	N/A	3.3AVDD	PIN 12
AVDDL	3.3AVDD	2.5AVDD	2.5AVDD	PIN 3/7/20/16
V_DAC	N/A	2.5AVDD	2.5AVDD	
DVDD	2.5VDD	1.8VDD	1.2VDD	PIN 24/32/45/54/64
DVDD_A	N/A	1.8AVDD	1.2AVDD	/78/99/110/116
				PIN 126

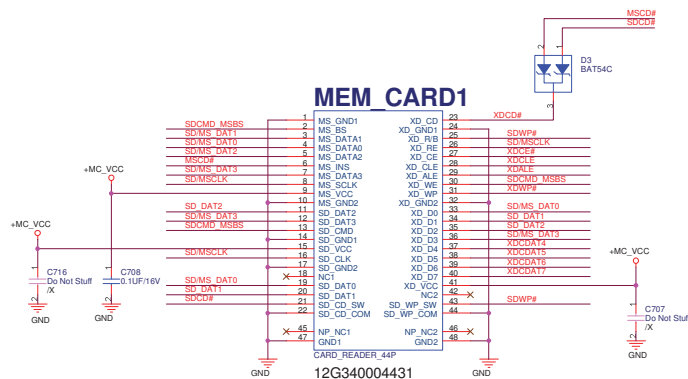
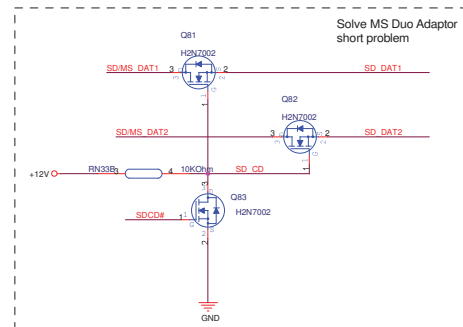
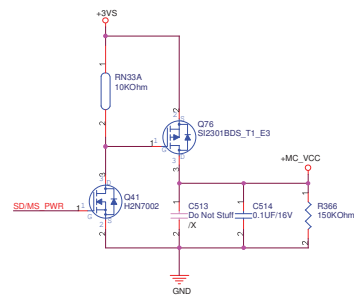


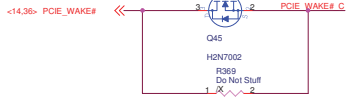
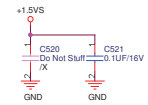
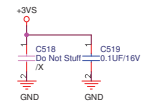
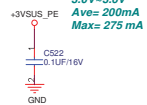
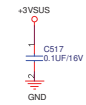
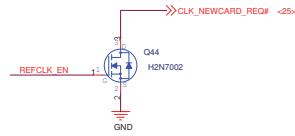
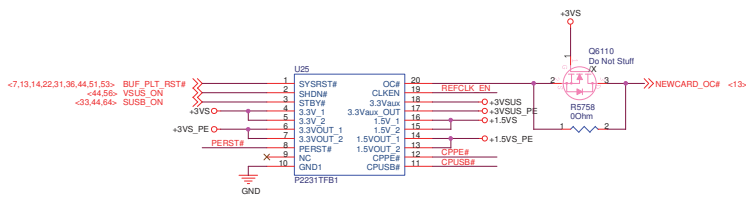
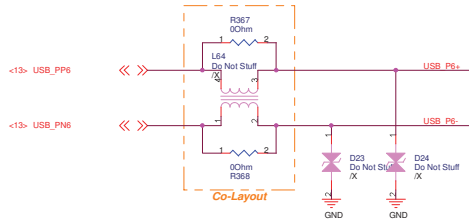




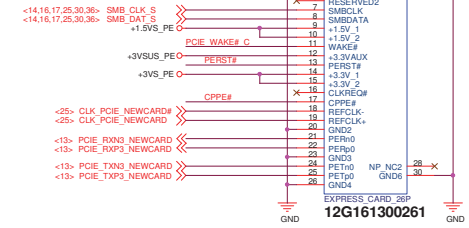


<< XDCDAT7 <3>
 << XDCDAT6 <3>
 << XDCDAT5 <3>
 << XDCDAT4 <3>
 << SDMS_DAT3 <3>
 << SDMS_DAT2 <3>
 << SDMS_DAT1 <3>
 << SDMS_DAT0 <3>
 << SDCMD_MBSBS <3>
 << XDWP# <3>
 << XDALE <3>
 << XDCLK <3>
 << XDCE# <3>
 << SDWP# <3>
 << SDCD# <3>
 << MSCD# <3>
 << SDMSCLK <3>
 << SDMS_PWR <3>





!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

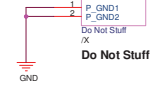


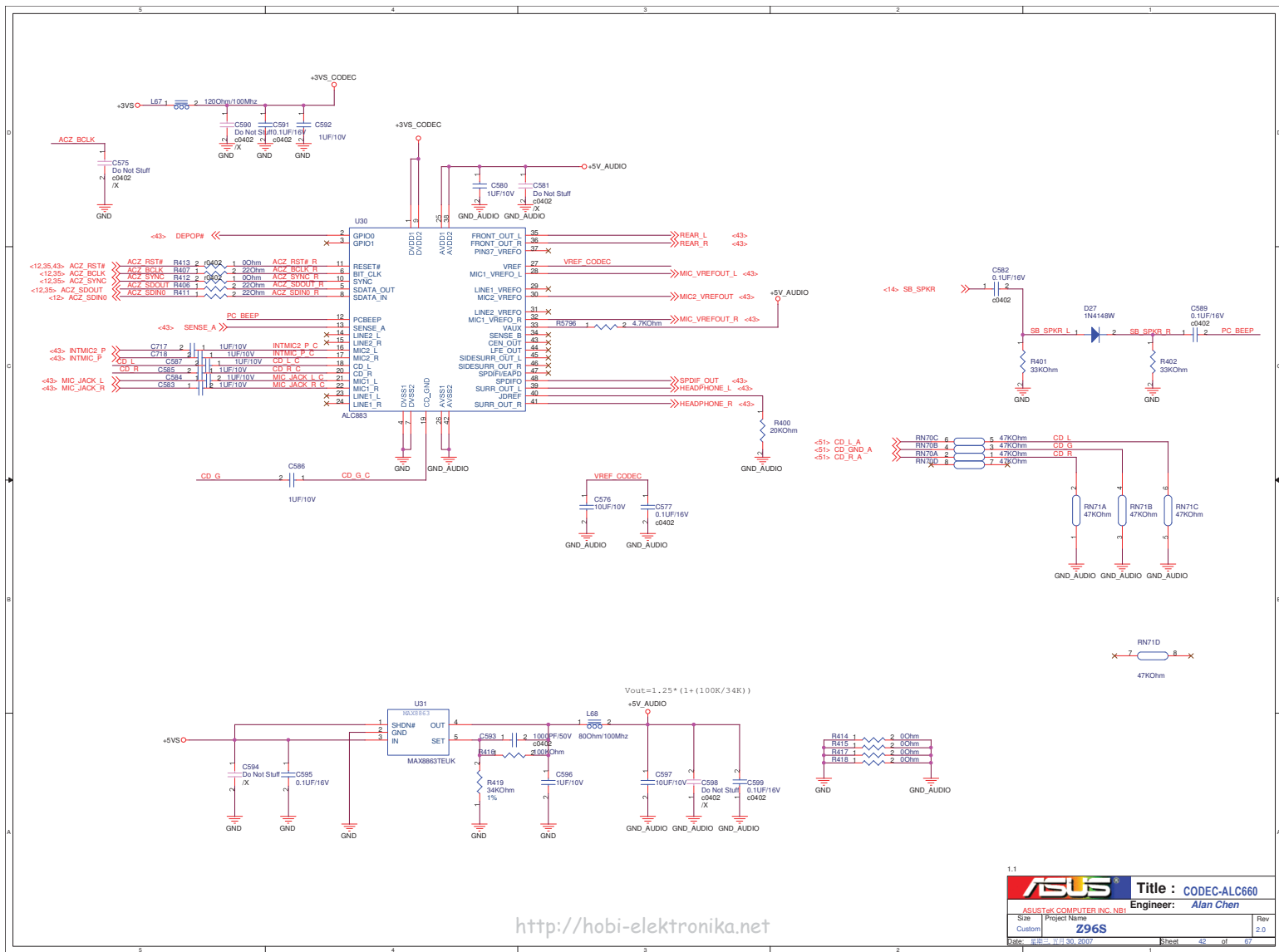
NewCard Header

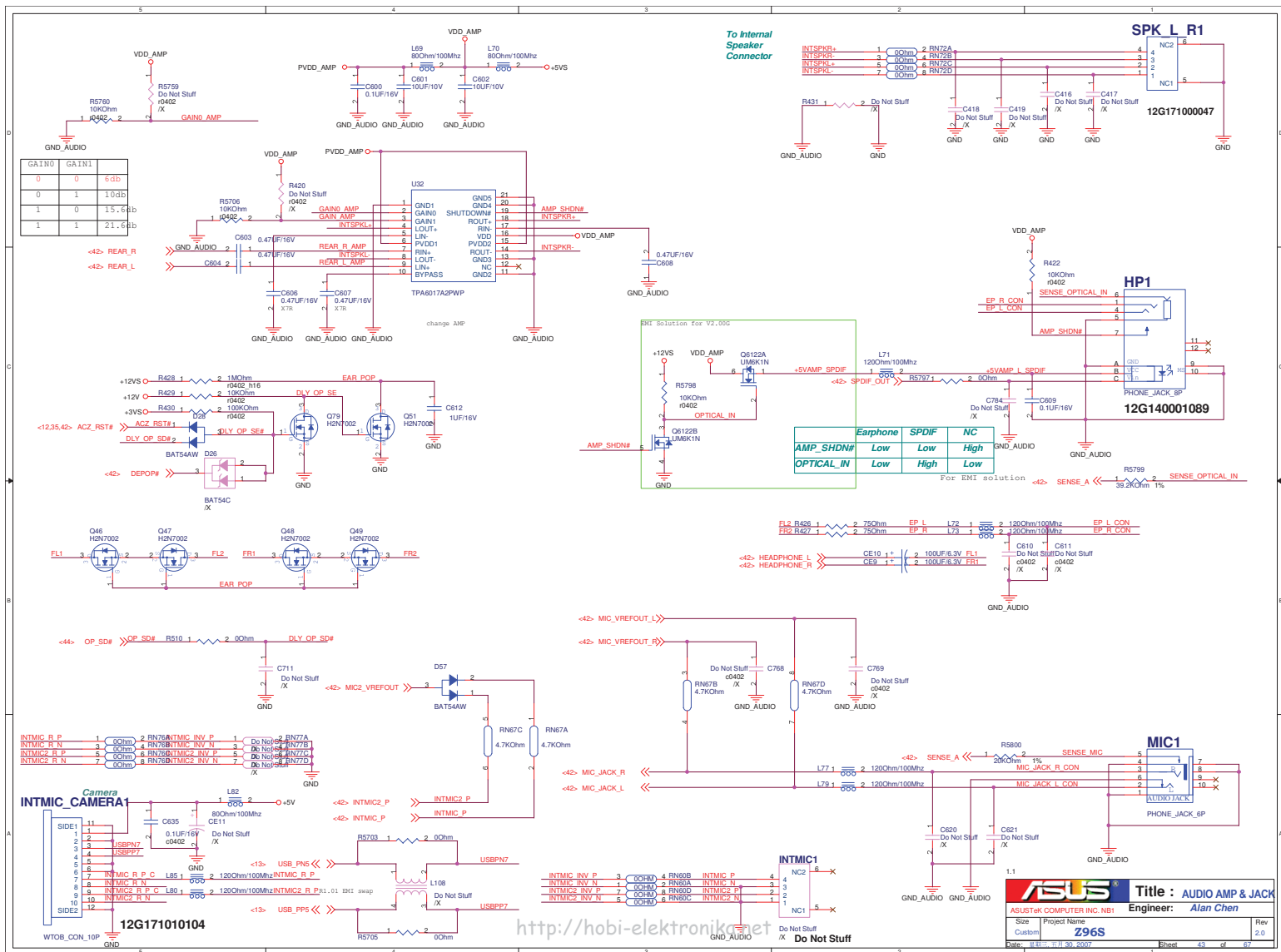
EXPRESS1

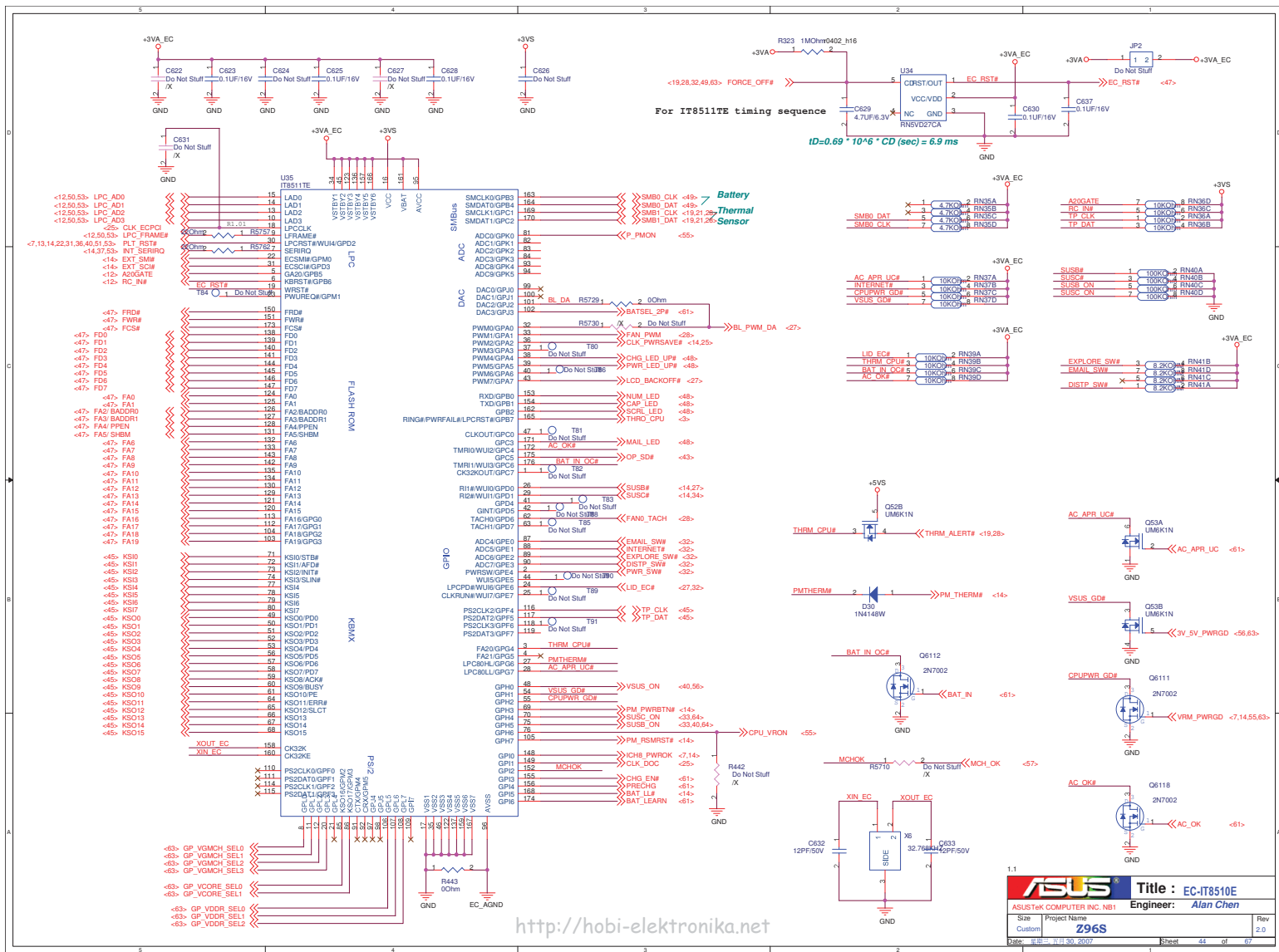
NewCard Ejector

EJECTOR1





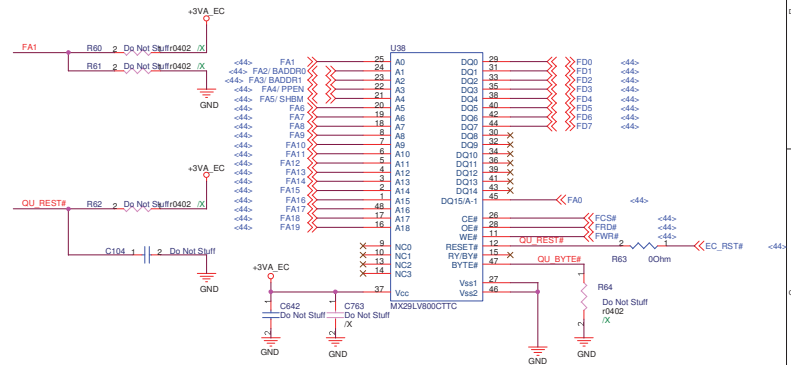
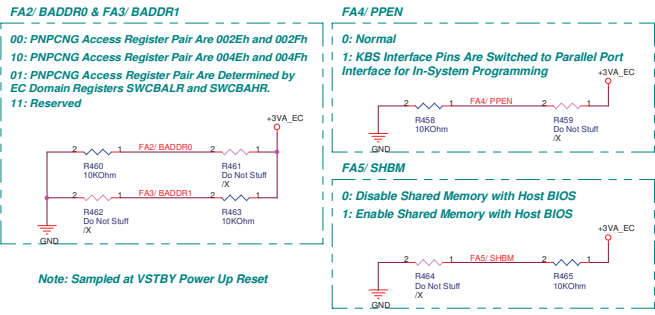






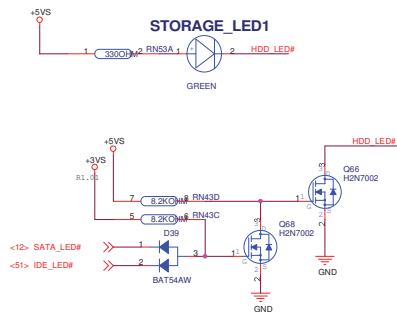
ISA ROM

EC Hardware Strapping

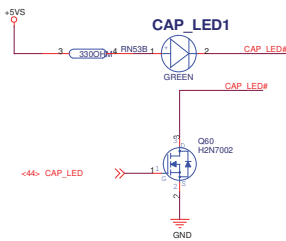


For LED

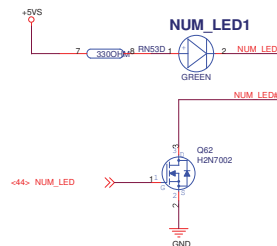
For SATA/IDE LED



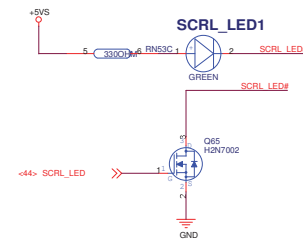
for Cap. Lock



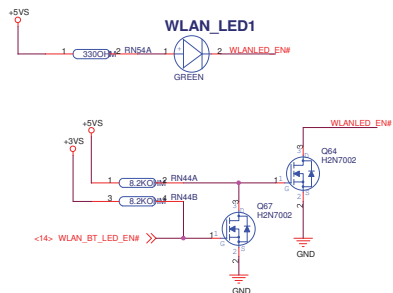
for Num Lock



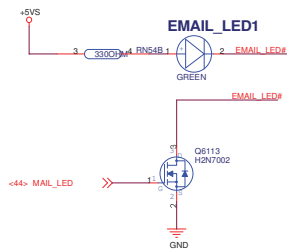
for Scroll Lock



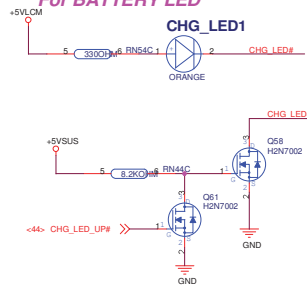
For WireLess LED



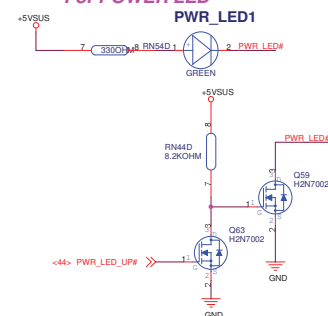
for email



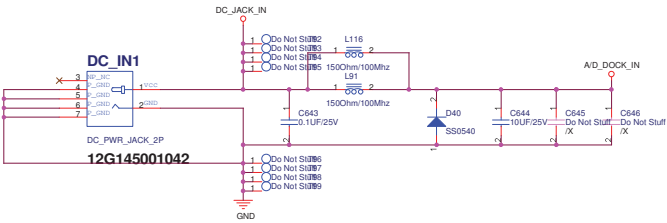
For BATTERY LED



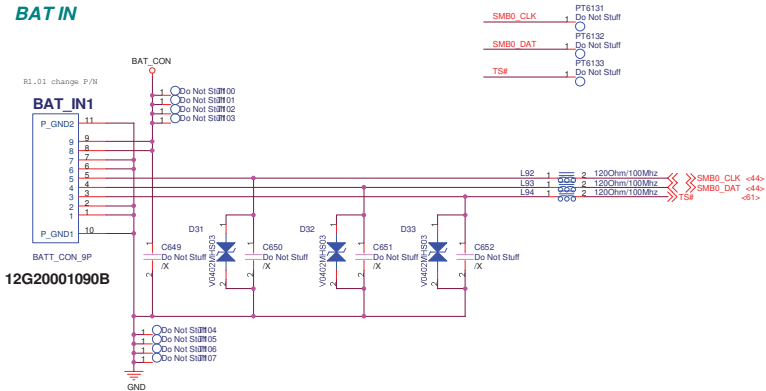
For POWER LED



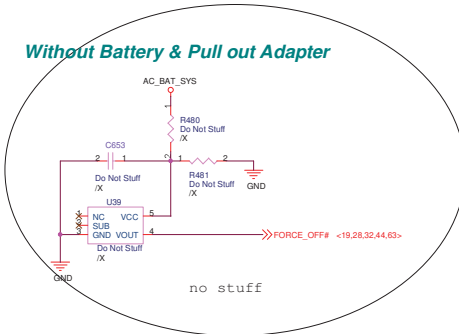
DC IN



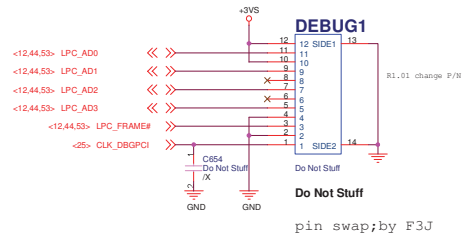
BAT IN

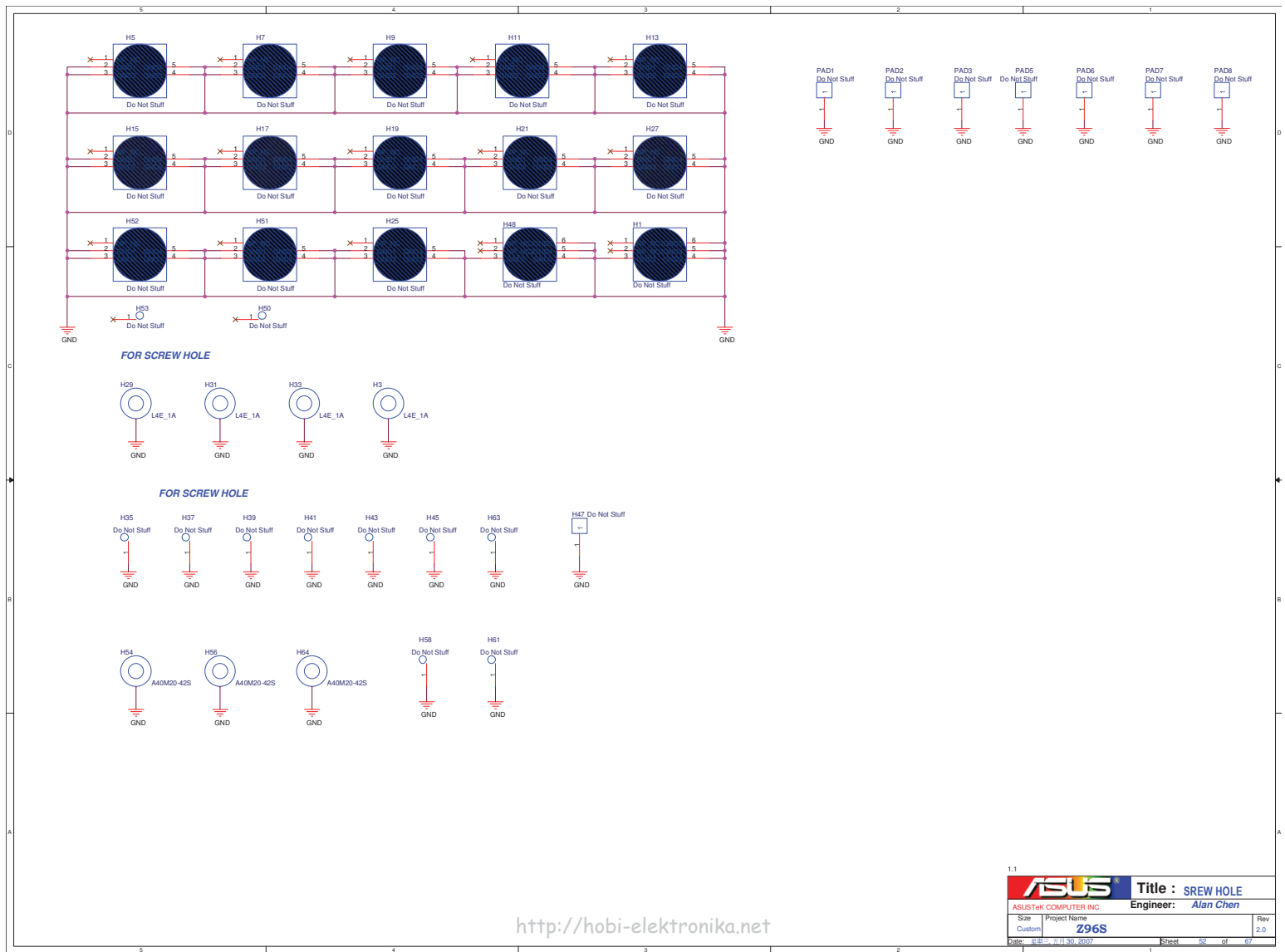


~~Without Battery & Pull out Adapter~~

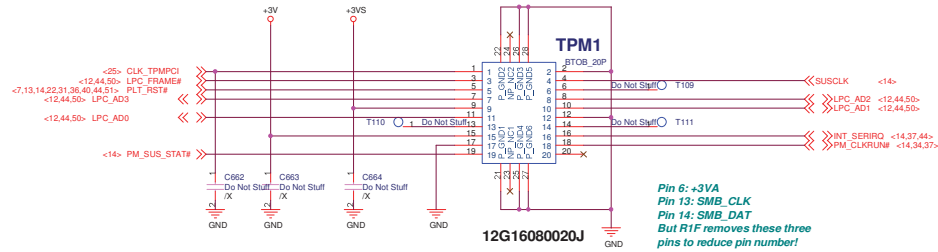


For Debug





For TPM Module

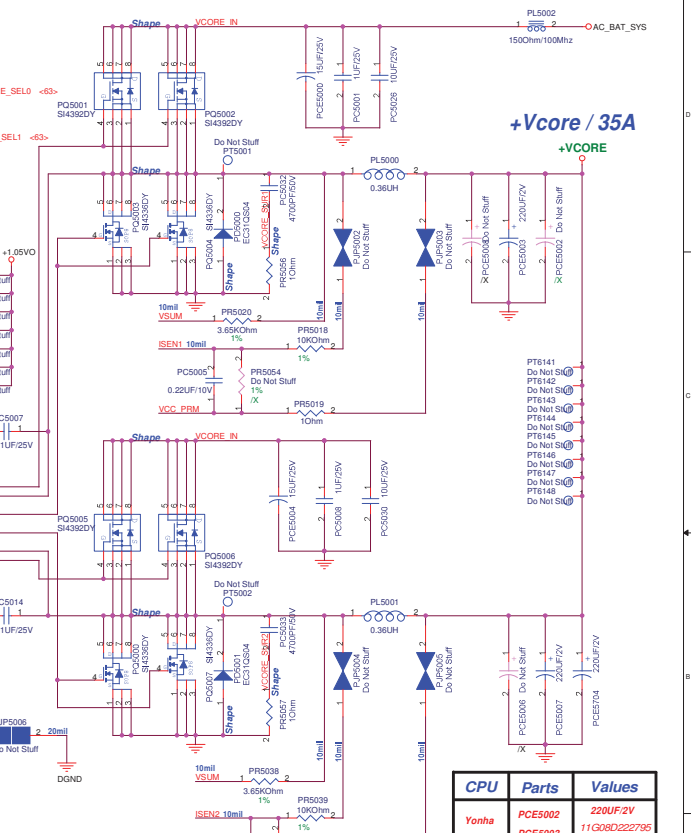
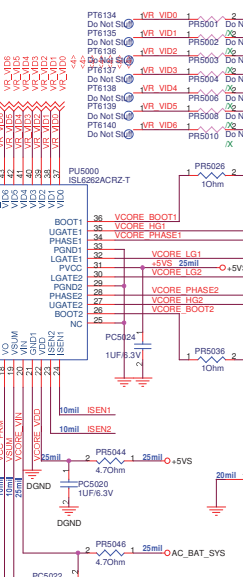
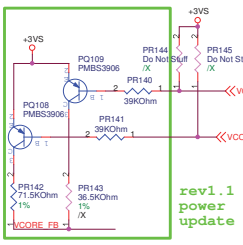
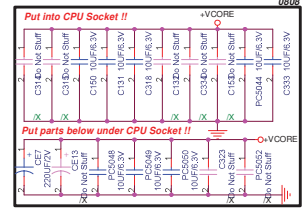
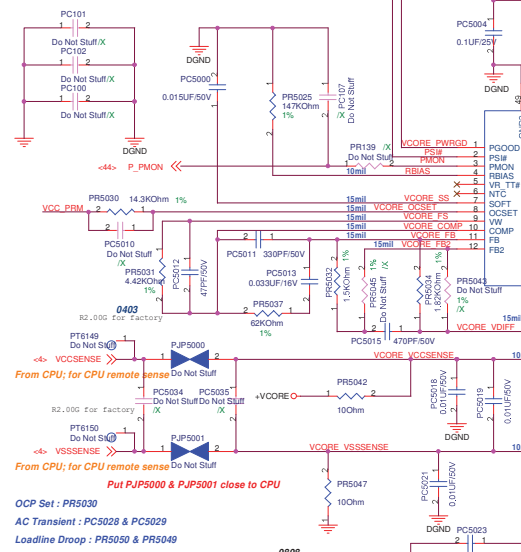


For Bluetooth



VCORE_SELO	VCORE_SEL1	Voltage
L	L	VID-150mV
X	L	VID-50mV
L	X	VID-100mV
X	X	VID

<<< CPU_VRON
CPU_VRON = 1, Vcore Regulator Enabled
<<< PM_DPRSLPVR
PM_DPRSLPVR = 1, CPU Deeper Sleep Mode is enabled
<<< STP_CPUH
STP_CPUH = 0, CPU is in Deeper Sleep Mode
<<< CLK_EN#
CLK_EN# = 0, Enable Clock Gen
<<< VIM_PWRGD
VIM_PWRGD = 1, Vcore Power OK
To N/B
PSM# = 0, Light Load (1-phase)
From CPU



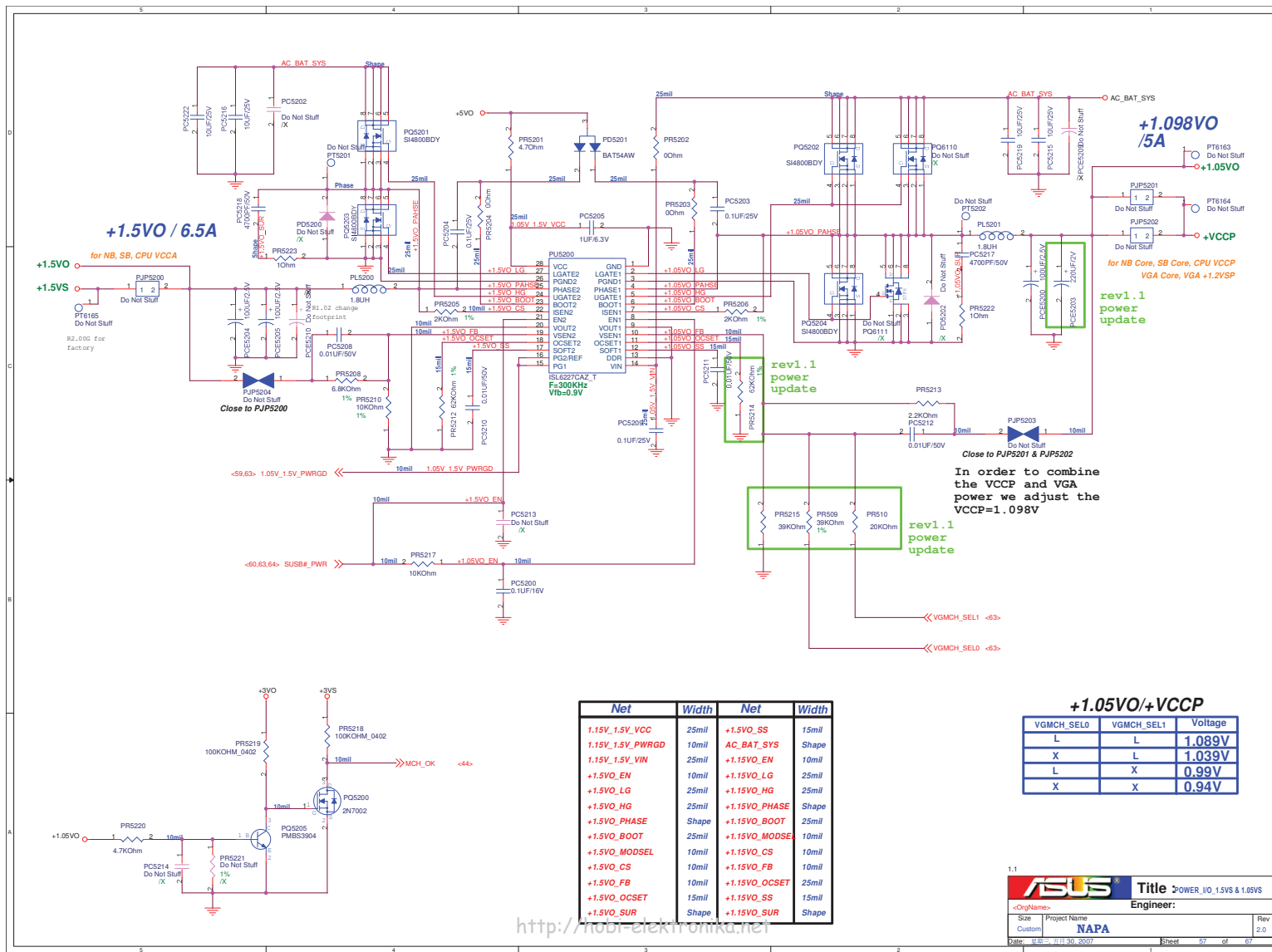
CPU	Parts	Values
Yonha	PCE5002	220UF/2V
	PCE5003	11G08D222795
Merom	PCE5006	330UF/2V
	PCE5007	11G08D337791

Net	Width	Net	Width
VR_V00 - VR_V06	10mil	DROOP & DROOP_FB	10mil
VR_ON & PS# & RBAS	10mil	VCC_PPM & VSUM	10mil
DPRSLPVR & DPRSTP	10mil	ISEN1 & ISEN2	10mil
VCORE_PWGRD	10mil	VCORE_VDD & _VIN	25mil
MCH_PWOK	10mil	VCORE_BOOT1	25mil
VR_TT# & NTC	10mil	VCORE_BOOT2	25mil
VCORE_SS & OCSET	15mil	VCORE_HG1 & HG2	25mil
VCORE_FS & _COMP	15mil	VCORE_LG1 & LG2	25mil
VCORE_FB & _FB2	15mil	VCORE_PHASE1	Shape
VCORE_VDIFF	15mil	VCORE_PHASE2	Shape
VCORE_VCSSENSE	15mil	VCORE_SUR1 & SUR2	Shape
VCORE_VDD	10mil	AC_BAT_SYS	Shape

ASUS Title: POWER.VCORE
Engineer:
Date: 2007-09-30
Rev: 2.0

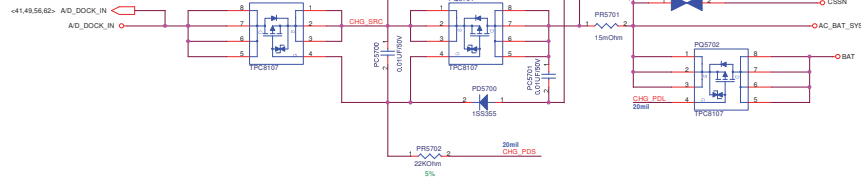


The diagram shows a timing sequence for three components: PT5110, PJP5102, and PT5111. The sequence starts with +5VAO, followed by a 'Do Not Stuff' region for PT5110, then a '1' (data bit), then a 'Do Not Stuff' region for PJP5102, then a '2' (data bit), then a 'Do Not Stuff' region for PT5111, and finally +5VA. The PJP5102 component is highlighted with a blue box containing '1 2'.





POWER PATH & BAT_LEARN



Charger shut down condition :

1. $V_{ictl} < 0.06V$
2. $PKPRES\# > 55\%$ of MAX8725_LDO
3. AC Adaptor Removed

The timing of PDL & PDS switch :

BAT - AD_DOCK_IN > 100mV -> Battery mode

The current capacity of MAX8725_LDO is 10mA.

VBAT_DLGV is a voltage for driving MOSFET.

MAX8725_AGIN < 10.27V, AC Adaptor absent
MAX8725_AGIN > 10.27V, AC Adaptor absent

MODE (Pn7)	Battery
High (-2.8V)	4 Cell
Low (-0.8V)	3 Cell
High Impedance (1.6V ~ Vmode-2V)	Battery Learn

MAX8725_REF : 4.2235V
MAX8725_LDO : 5.4V

Battery Charging Voltage :
 $+V_{BAT} = 3 \times [4.2235 + (V_{vcl} - 1.8) / 9.52]$

Battery Charging Current :
 $I_{charge} = (0.075 / PR5706) \times (V_{ictl} / 3.6)$

Input Adaptor Max. Current Limit :
 $I_{limit_current} = (0.075 / PR5701) \times (V_{icls} / 4.2235)$

Pre-Charging Mode :

Precharging current = 150 ~ 160mA
 $V_{ictl} = 0.100V - 0.120V$

Battery Cell Selection :

BATSEL_2P# = 1, 6 Cells; $V_{ictl} = 2.084V$ CHG_EN# = 0, Charger Enabled
=> $I_{charge} = 2.894A$
BATSEL_2P# = 0, 9 Cells; $V_{ictl} = 3.219V$ CHG_EN# = 1, Charger Enabled
=> $I_{charge} = 4.472A$

Adaptor Max. Current :

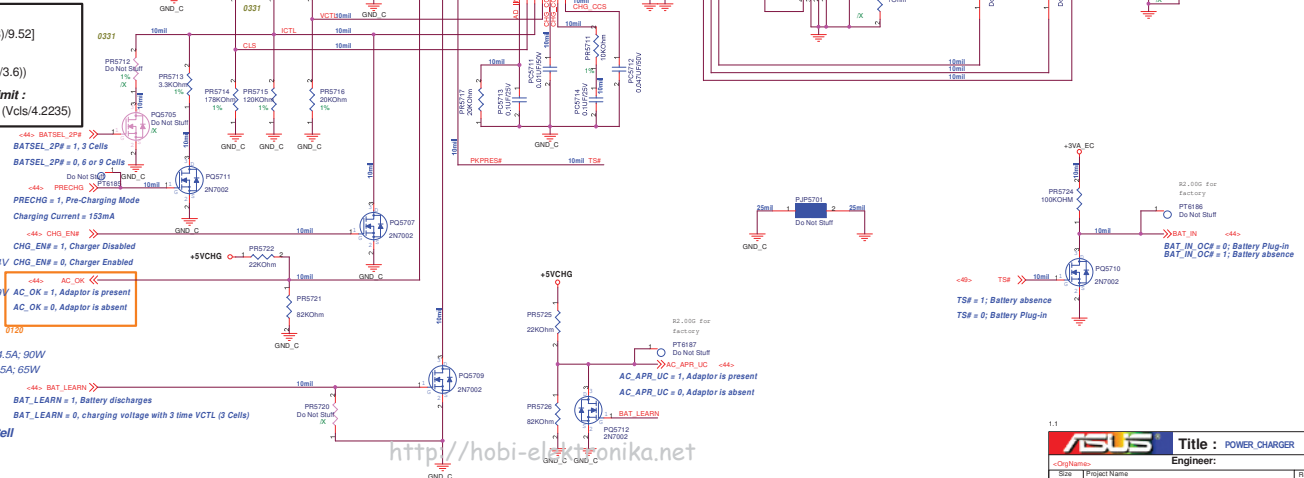
PR5714 = 178K; $V_{ids} = 3.79V$, $I_{limit} = 4.5A$; 90W
PR5714 = 47K; $V_{ids} = 2.96V$, $I_{limit} = 3.5A$; 65W

BATSEL_SP# = 1, 3-Cell

$V_{ictl} = 1.22V$; $I_{charge} = 1.69A$

BATSEL_SP# = 0, 6-Cell or 9-Cell

$V_{ictl} = 2.11V$; $I_{charge} = 2.93A$



for EMI requirement

EC6109, EC6110, Do Not Stuff, Do Not Stuff

0302 for EMI requirement

82.05 50K, Do Not Stuff

82.05 50K, Do Not Stuff

82.05 50K, Do Not Stuff

82.05 50K, Do Not Stuff

82.05 50K, Do Not Stuff

82.05 50K, Do Not Stuff

82.05 50K, Do Not Stuff

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82.05 50K, Do Not Stuff

82.05 50K, Do Not Stuff

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82.05 50K, Do Not Stuff

82.05 50K, Do Not Stuff

82.05 50K, Do Not Stuff

82.05 50K, Do Not Stuff

82.05 50K, Do Not Stuff

82.05 50K, Do Not Stuff

82.05 50K, Do Not Stuff

82.05 50K, Do Not Stuff

82.05 50K, Do Not Stuff

<http://hobi-electronics.com>

1.1



1.1



Title : POWER_DETECT

<OrgName>

Size

et Name

NAPA

Rev

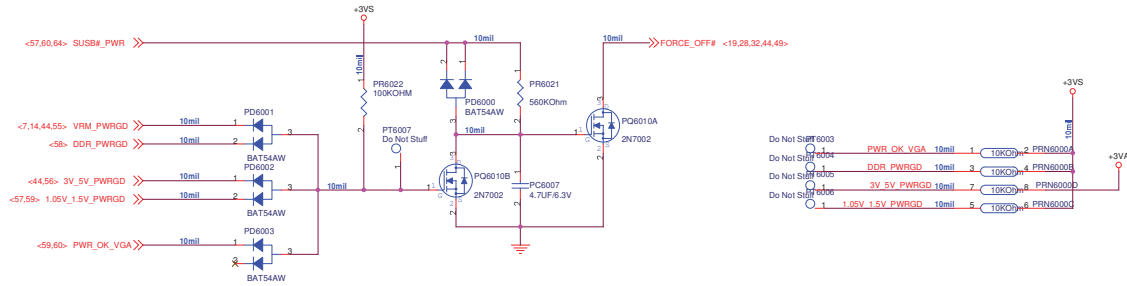
2.0

Date: 星期三, 五月 30, 2007

Sheet 62 of 67

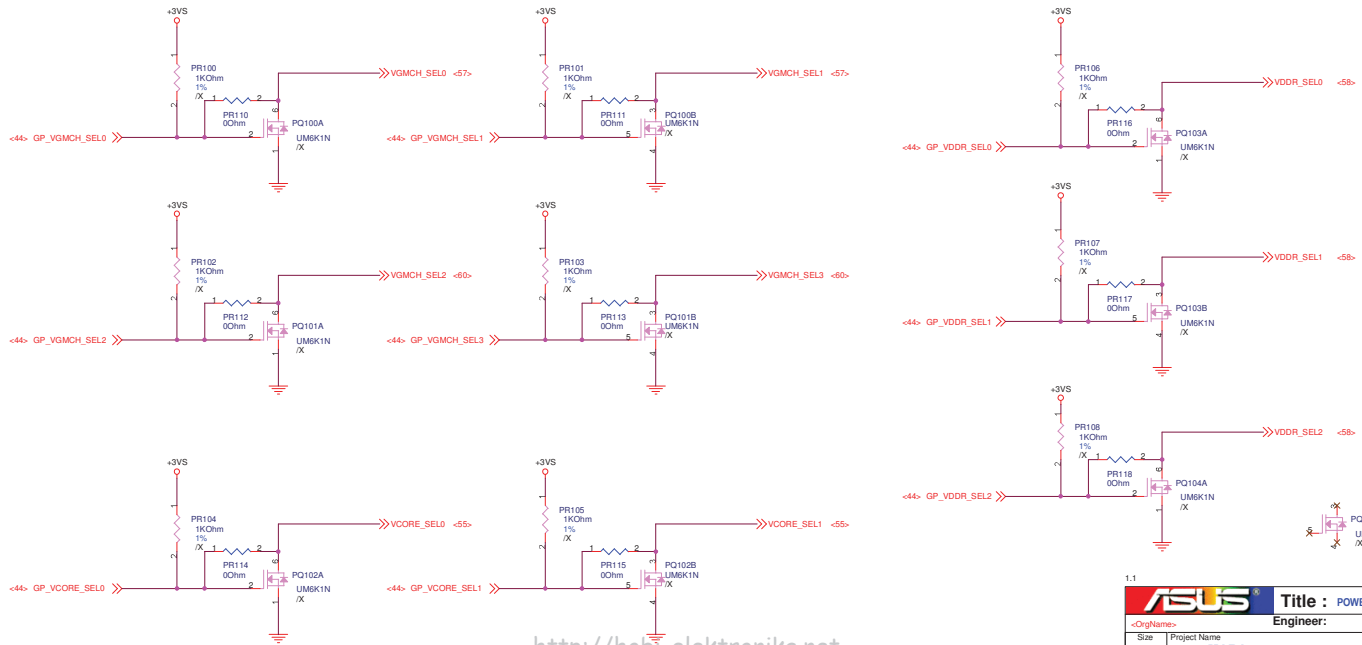
	2013-14	2014-15	2015-16	2016-17	2017-18
1. Revenue	100.00	100.00	100.00	100.00	100.00
2. Capital	100.00	100.00	100.00	100.00	100.00
3. Debt	100.00	100.00	100.00	100.00	100.00
4. Grants	100.00	100.00	100.00	100.00	100.00
5. Other	100.00	100.00	100.00	100.00	100.00
6. Total	100.00	100.00	100.00	100.00	100.00

Power Good Detector

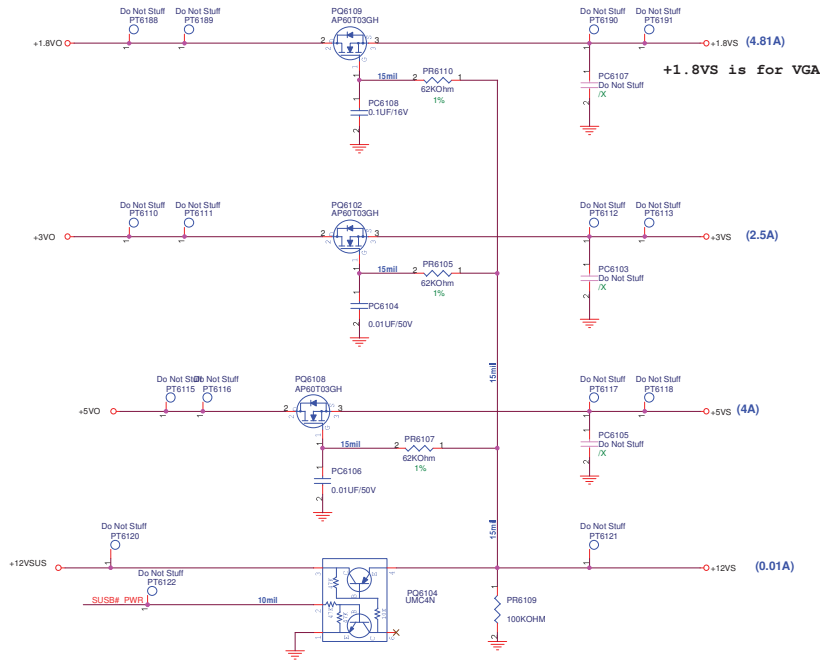


Power Voltage control

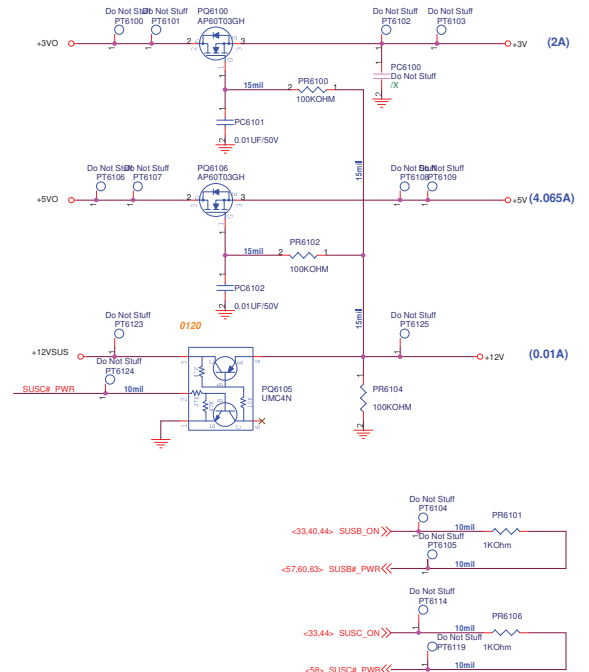
Modify V2.0G

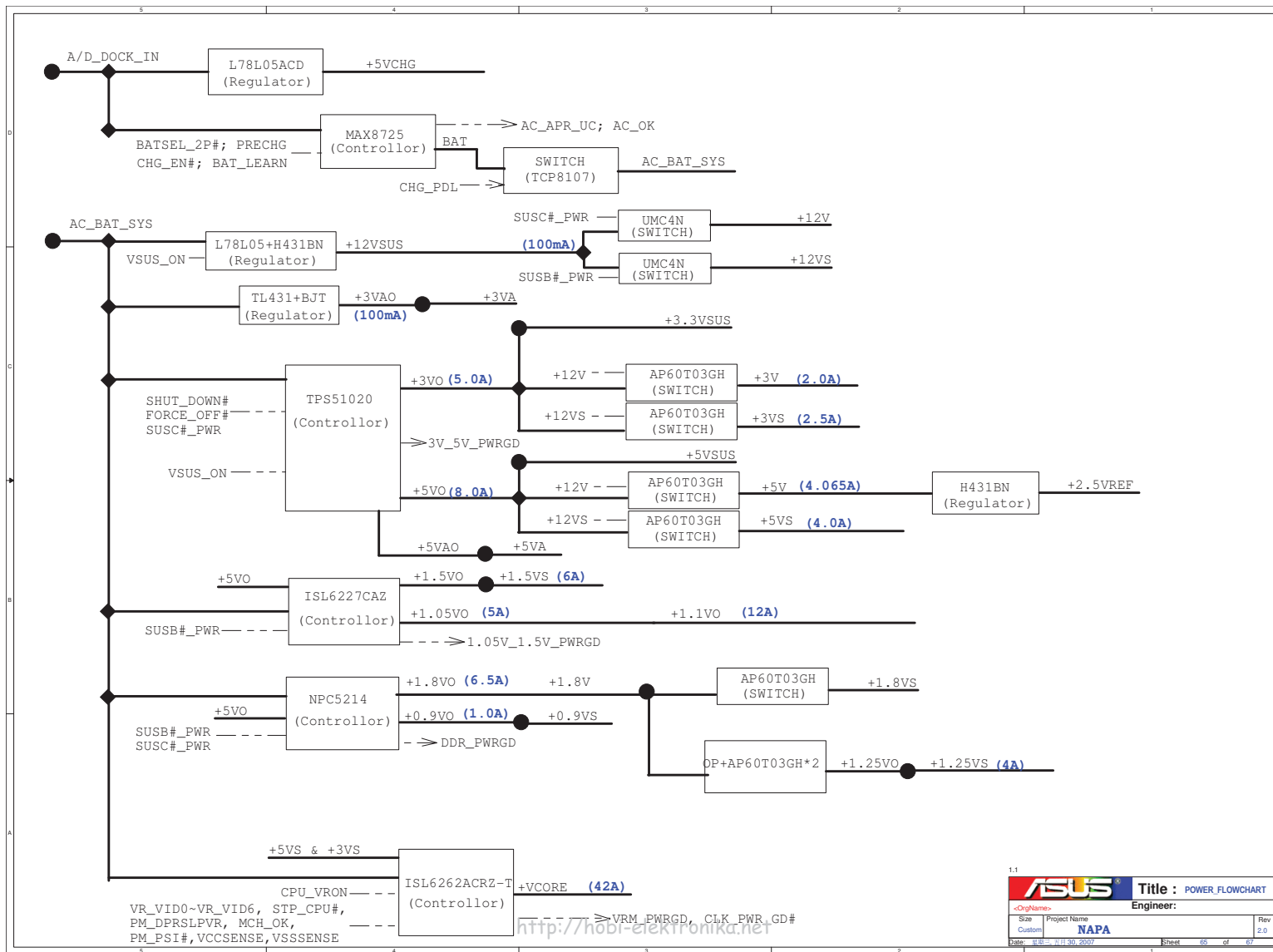


SUSB#_PWR POWER



SUSC#_PWR POWER





1.1

		Title : POWER_FLOWCHART	
<OrigName>		Engineer:	
Size Custom	Project Name NAPA		Rev 2.0
Date: 2007-11-30	Sheet: 65 of 67		



